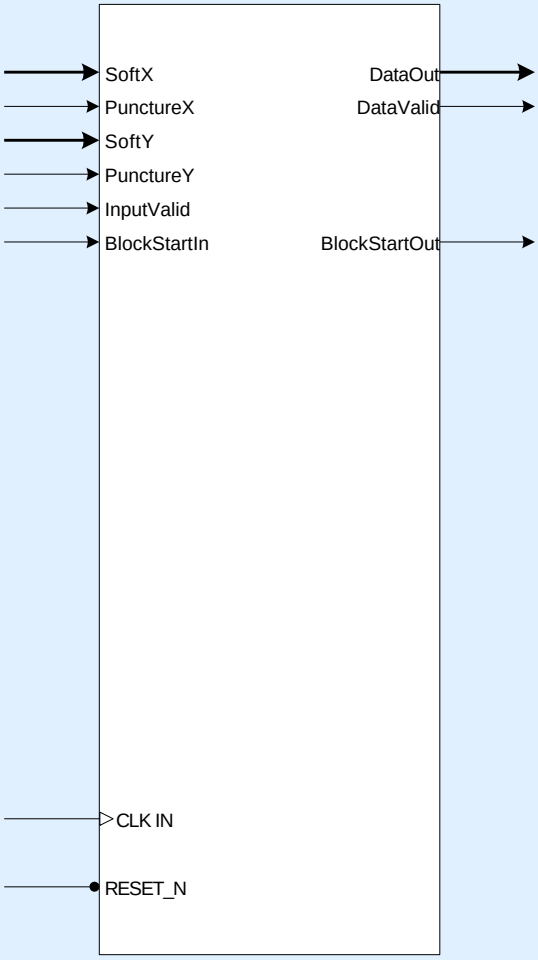
(Tail-biting) Viterbi Decoder

CMS0008

- Advanced Tail-Biting Architecture yields high coding gain and low delay.
- Synthesis configurable code generator coefficients and constraint length, soft-decision width and codeblock size.
- User-defined puncture patterns.
- Flexible memory architecture suitable for FPGA or ASIC.



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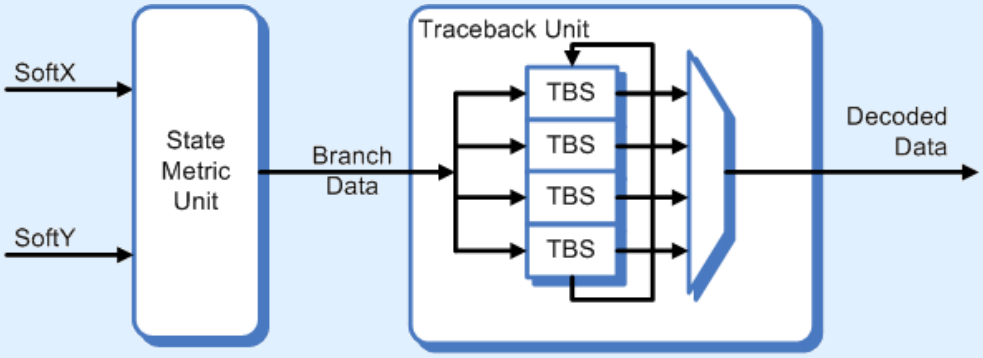
Block Diagram



Detailed Description

The Commsonic CMS0008 Viterbi Decoder core implements Viterbi's algorithm for maximum likelihood decoding of non-feedback convolutional codes.

The basic 1/2 rate convolutional encoder and decoder are shown above. For each input bit, two encoded bits are produced. The rate can be increased to 2/3, 3/4, 5/6, or 7/8 by non-transmission (puncture) of certain bits. Punctured codes lose coding gain as the redundant content decreases.

The encoded X and Y bits are transmitted through a noisy channel. The received X and Y values are measured then presented as soft decision values to the decoder.

A description of the processing steps follows:

State Metric Unit. This block maintains a measure of probability for each possible encoder state. As each soft pair is processed, the SMU produces the most likely received data bit for each state (the Branch Data vector).

Traceback Unit. This block provides a history of most likely state transitions. This allows traceback from any current state to ever more likely predecessor states. After a certain depth the optimum state becomes known and traceback from this point produces reliable data. The required minimum traceback depth depends on the code parameters, puncture rate and soft-decision width.

Burst-Mode Operation

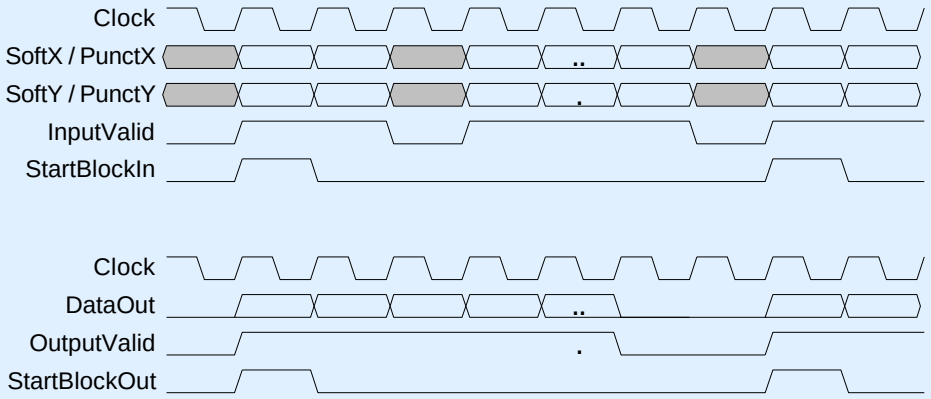
Convolutional codes are fundamentally continuous processes and their use in burst-mode systems is problematic.

Many burst mode systems specify the use of known start- and end-states (typically zero) to correctly terminate the discontinuous data stream. However this requires insertion of non-payload termination symbols into the data stream, consuming valuable bandwidth.

The alternative tail-biting strategy places data in the termination symbols, increasing the payload size at the cost of some additional decoder complexity.

While the additional complexity might seem daunting, the actual cost penalty is not high. Our tail-biting decoder provides comparable coding gain and group delay to typical zero-terminated decoders, with a moderate increase in gate count.

Decoder Timing Diagram



Notes,

1. Data is transferred on cycles when InputValid = 1. The input data stream may be discontinuous.
2. Each output codeblock is a continuous stream of bits, occurring a fixed delay after the last soft decision input.
3. Data is transferred out on cycles when OutputValid = 1.
4. It is not necessary to have null cycles between codeblocks; they may be processed in a continuous bit-per-clock data stream.

Principle I/O Description

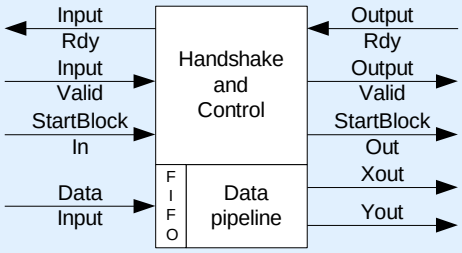
Datapath Inputs	
SoftX	X and Y decoder soft decision inputs. 0000 => strong 0, 1111 => strong 1
SoftY	
PunctureX	These signals indicate that the corresponding SoftX or SoftY input has been punctured from the code. The state metric unit removes that soft decision from the maximum-likelihood calculation. External logic must provide the puncture pattern.
PunctureY	
InputValid	Indicates clock cycle on which soft data and puncture inputs are valid.
Frame Control	
BlockStartIn	Indicates first input sample of code block.
Outputs	
DataOut	Decoded data
DataValid	Indicates clock cycle on which decoded data is valid
BlockStartOut	Indicates first output bit of code block.

Synthesis Controls

ConstraintLength	Constraint length of the convolutional code = log2(states)+1 = state_shift_register_length+1
Gx	Defines convolutional encoder x output as function of state
Gy	Defines convolutional encoder y output as function of state
SoftLength	Bit width of SoftX and SoftY inputs
CodeblockSize	Size of codeblock = traceback length

Encoder Operation

To support bi-directional flow control, the encoder block implements bi-directional handshaking signals. Data transfer occurs on clock cycles when both Rdy and Ack are valid.



Datapath Inputs	
DataIn	Uncoded input data bits
Datapath Outputs	
Xout	X and Y encoder outputs
Yout	
Dataflow Control	
InputValid	Input indicating clock cycle on which data input is valid
InputRdy	Output indicating input buffer is ready to accept uncoded input data
OutputRdy	Input indicating next block is ready to accept encoded output data
OutputValid	Output indicating clock cycle on which encoded data outputs are valid
Frame Control	
StartBlockIn	Indicates first input sample of code block.
StartBlockOut	Indicates first output sample of code block.

Synthesis Controls

ConstraintLength	Constraint length of the convolutional code = log2(states)+1 = state_shift_register_length+1
Gx	Defines convolutional encoder x output as function of state
Gy	Defines convolutional encoder y output as function of state
BlockSize	Bits per codeblock = traceback length

About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/S2/DSNG, DVB-C/J.83/A/B/C, DVB-T/H, DVB-T2, ATSC and ISDB-T.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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