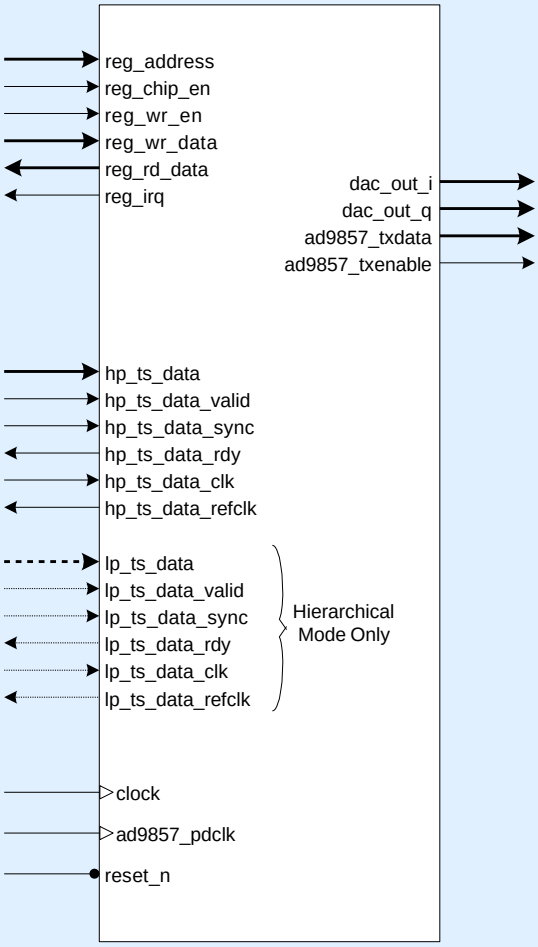
DVB-T/DVB-H Modulator

CMS0009

- Fully compliant with ETSI EN 300 744 V1.5.1.
- Extension core available for DVB-T(H) support.
- Enables rapid development of audio/visual systems using commodity Free-to-Air set-top-box technology and low-cost FPGAs.
- Configurable support for 2K and 8K OFDM modes and hierarchical transmission. (4k for DVB-T(H))
- Variable channel bandwidth support using a single clock reference; 5MHz… 8MHz.
- AD9857/AD9957/AD9789 interface and auto-programming support.
- AD9516/ADF4350 PLL programming support.
- Optional dual-core combining into the AD9857 for multi-channel applications.
- Extension core available for SPI/ASI interface with integrated PCR TS re-stamping, NULL TS packet removal/filtering, NULL/PRBS TS packet insertion, input and output TS rate estimation registers.
- Seamless integration with Altera ASI megacore when using SPI/ASI extension core.
- Optional FFT output windowing.
- Optional critical-mask output filtering.
- Optional in-band or output pre-distortion.
- Optional noise interference source
- Modes that are not required may be removed with synthesis options to generate a compact, efficient design.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).



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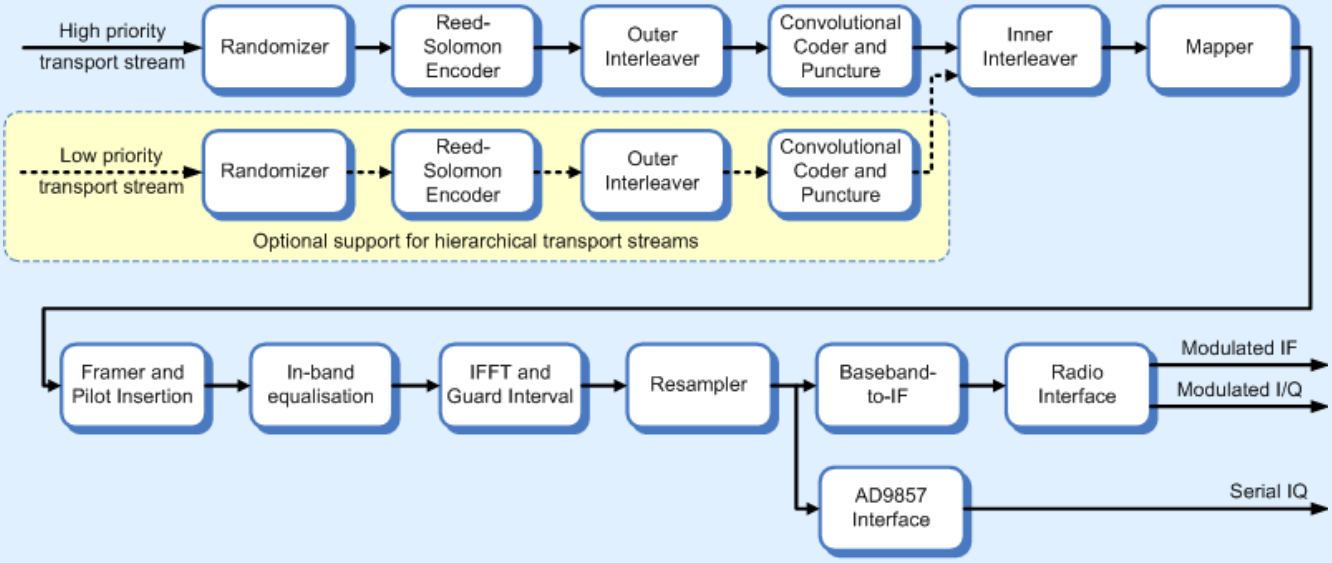
Block Diagram



Detailed Description

The Commsonic CMS0009 DVB-T/DVB-H Modulator provides all the necessary processing steps to modulate a single (or pair of hierarchical) transport stream(s) into a complex I/Q signal for input to a pair of DACs, or an interpolating DAC device such as the AD9857 or AD9957. Optionally the output can be selected as an IF to supply a single DAC.

The design has been optimised to provide excellent performance in low cost FPGA devices such as the Cyclone™ range from Altera or the Spartan™ range from Xilinx

A description of the processing steps follows:

Randomiser. This block performs the energy dispersal and transport multiplex adaptation using the DVB randomisation polynomial $1+x^{14}+x^{15}$ and also by inverting every eighth sync byte.

Reed-Solomon Encoder. This block generates Reed Solomon packets based on the DVB RS(204, 188) code with code generator polynomial:

$$g(x) = (x+\lambda^0)\,(x+\lambda^1)\,(x+\lambda^2)\ldots\,(x+\lambda^{15})$$

Where λ = 0x02, and field generator polynomial:

$$p(x) = x^8 + x^4 + x^3 + x^2 + 1$$

Outer Interleaver. This block performs the DVB outer interleaving function with depth I=12 as specified by the DVB standard.

Convolutional Encoder. This block performs the convolutional encoding as specified by DVB.

Interleaver. DVB-T specifies a block based bit interleaver concatenated with a symbol interleaver in a two-step process. If a hierarchical system is selected then the two streams are merged at this point using a modified interleaving equation. The DVB-T(H) extension core provides in-depth interleaving as required..

QAM Mapper. This block performs the QAM constellation mapping using the mapping schemes specified by DVB for QPSK, QAM16 or QAM64. It outputs I/Q QAM symbols to the IFFT core.

Framer. The DVB-T specification details a frame and super-frame structure with scattered, continuous and TPS pilots inserted at various carriers within each symbol. This block manages the pilot insertion dependent on the selected mode (2k, 4k or 8k), and symbol position within a frame. Note that the full system can be switched via software register (or hardware port) to use 2k, 4k or 8k mode. Alternatively a reduced memory 2k-only mode may be synthesised.

In-band equalisation An optional in-band equalizer circuit may be specified as a synthesis option. This allows the designer to easily compensate minor phase and gain slope associated with linear filter components on the board.

Detailed Description (cont'd)

IFFT. This block performs the Inverse Fast Fourier Transform (IFFT) on the 2k, 4k or 8k carriers. A proprietary architecture is used which yields low Guassian noise, high MER outputs yet utilises low datapath widths. The IFFT also manages the on-air timing of the OFDM symbols by guard interval insertion. An optional windowing function is also included to reduce spurious emissions caused by the OFDM symbol transitions. A further optional non-linear pre-distortion can also be performed.

Resampler. This block resamples the 9·14MHz complex samples output from the IFFT into complex samples at the core clock frequency. This provides an ultra-flexible clocking strategy. This block also scales automatically as required to satisfy the selected channel bandwidth.

Baseband-to-IF. This block provides the option to mix the signal up to a higher IF as defined by a software register. This block may be removed using synthesis options if it is not required.

DAC Aperture Correction. This optional processing step provides compensation for the sin(x)/x (or SINC) distortion that is introduced in the DAC. This block may be removed using synthesis options is the feature is not required

Radio Interface. This block performs some final, register-selectable processing functions to optimise the output for the radio in the target application. For example, the data can be formatted to work with either twos-complement or offset-binary DAC devices. In addition the data is formatted to suit the external vice that could take separate I/Q, multiplexed I/Q or a single IF output.

Additional modes are added to support the Analog Devices AD9857 device that provide up-conversion, SINC filtering and DAC functions in a single package. The AD9857 device requires that the I/Q data be multiplexed onto a single data bus. The *ad9857_pdclk* input is provided to enable this feature and should be sourced from the AD9857 PDCLK output.

Register Bank. The register bank provides a simple 32-bit interface for reading and writing registers within the modulator block. Full details of the registers within the modulator core are contained within the full data sheet.

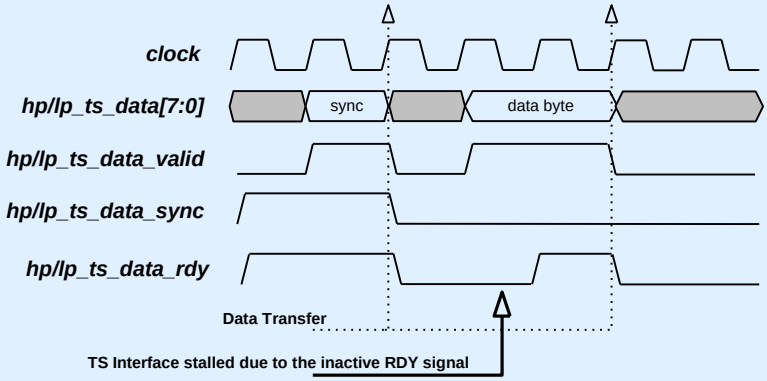
Principle I/O Description

Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0009 register bank.
reg-wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
Transport Stream Interface	
hp_ts_data	8-bit High Priority Transport Stream data input
hp_ts_data_valid	High Priority Transport Stream data valid input.
hp_ts_data_sync	High Priority Transport Stream data sync input.
hp_ts_data_rdy	High Priority Transport Stream path is ready for new byte. Data transferred when Ready and Valid are asserted together.
hp_ts_data_clk	High Priority Transport Stream clock input.
hp_ts_data_refclk	High Priority Transport Stream reference clock output.
lp_ts_data	8-bit Low Priority Transport Stream data input.
lp_ts_data_valid	Low Priority Transport Stream data valid input.
lp_ts_data_sync	Low Priority Transport Stream data sync input.
lp_ts_data_rdy	Low Priority Transport Stream path is ready for new byte. Data transferred when Ready and Valid are asserted together.
lp_ts_data_clk	Low Priority Transport Stream clock input.
lp_ts_data_refclk	Low Priority Transport Stream reference clock output.
Modulator Output Interface	
dac_out_i	14-bit Transmit I complex output or IF output in IF mode.
dac_out_q	14-bit Transmit Q complex output.
ad9857_txdata	14-bit multiplexed data to the AD9857 if used.
ad9857_txenable	Controls the interface timing to the AD9857 if used.
Others	
clock	Clock input, greater than 64MHz for 8k-mode operation.
ad9857_pdclk	AD9857 Clock.
reset_n	Asynchronous active-low reset input.

Transport Stream Interface

Standard TS interface:

The standard TS interface supplied uses a ready/valid handshake mechanism to allow data to be pulled through the modulator processing chain based on the on-air symbol rate. This requires the TS data source to be stalled when the modulator core is busy.

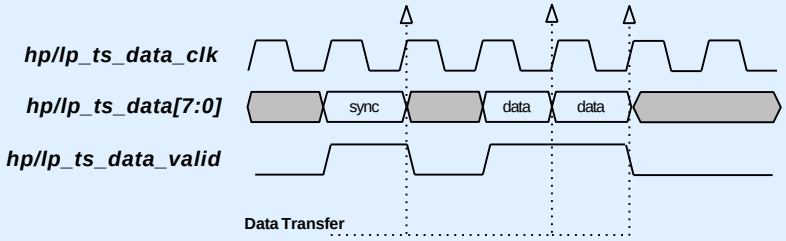


PCR re-stamping TS interface:

In certain applications it may be that the input stream from the transport multiplexer is provided at a fixed rate and will not support the standard TS interface handshake mechanism and consequently some form of rate adaption is required. The TS PCR restamping extension core provides a simpler TS interface (compatible with SPI or ASI) to allow data to be input at any rate.

The core will be pad the input TS stream with NULL TS packets (or PRBS TS packets) as required and perform any PCR adjustment.

When the PCR restamping extension core is used, an output signal, *hp_ts_data_refclk (lp_ts_data_refclk)* is provided that indicates the necessary 188-byte TS byterate to satisfy the OFDM on-air requirements.

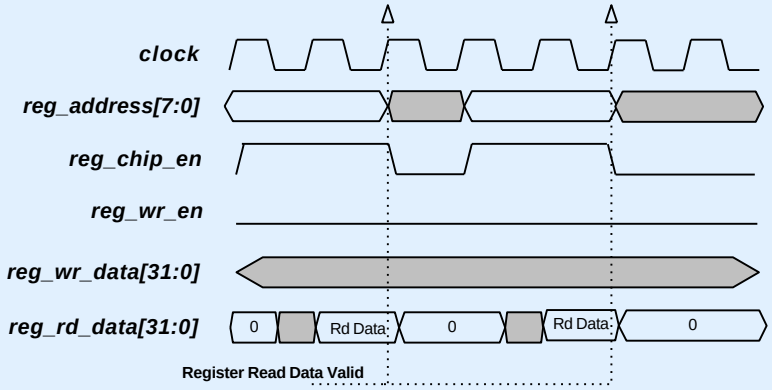


Register Interface

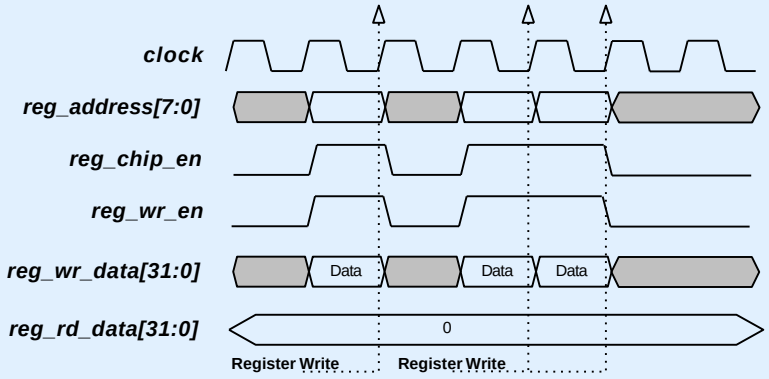
A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

An active-high interrupt line is also available.

Register read access:



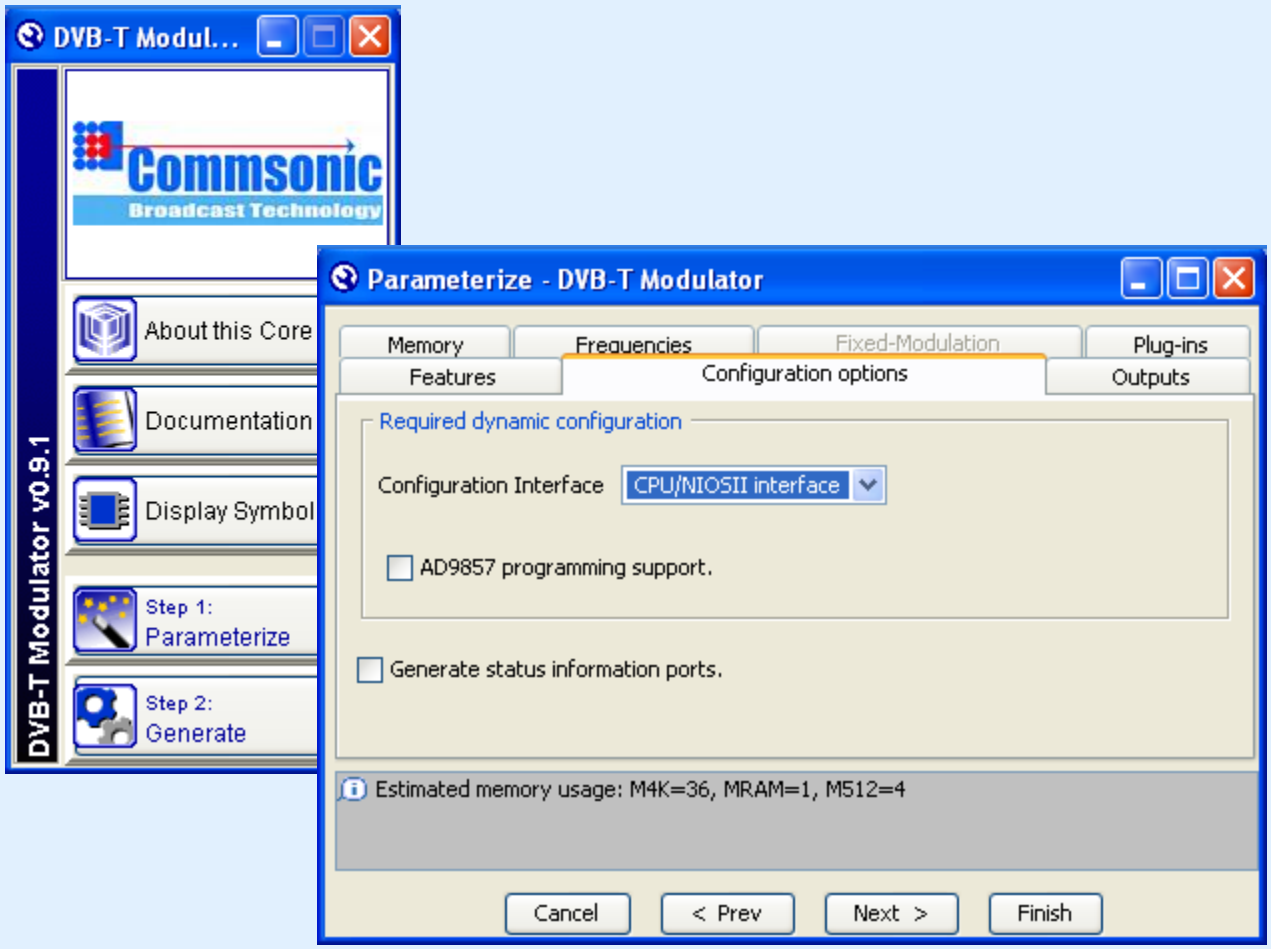
Register write access:



Altera® Megacore®

AMPP℠ Approved | OpenCore® Support | Qsys Compliant

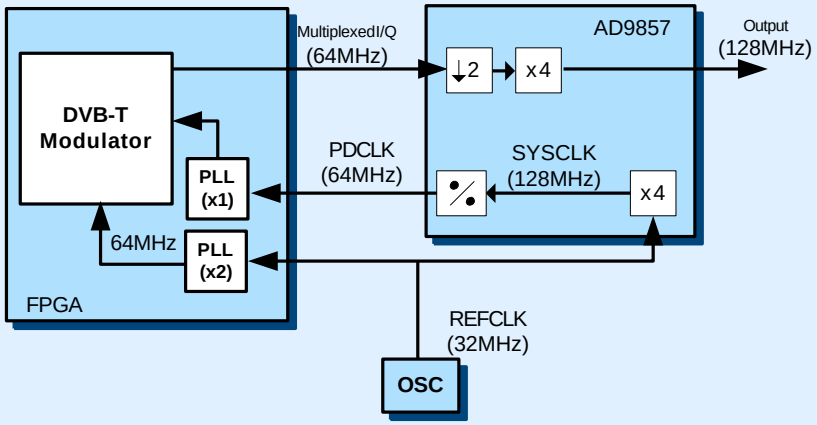
The DVB-T/DVB-H Modulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.



Example Applications

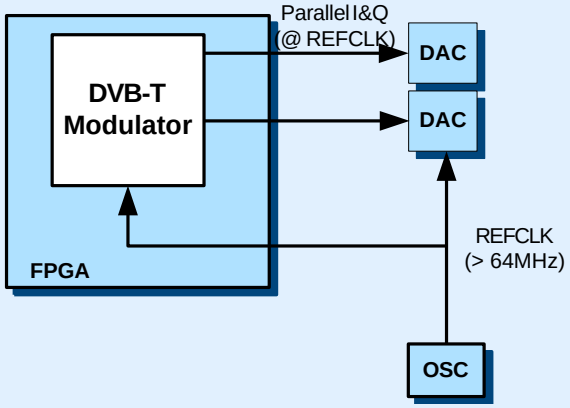
Up-sampled IFFT output using external up-conversion:

This application uses the DVB-T modulator core with internal interpolation that allows the channel bandwidth to be changed via a simple s/w register change.



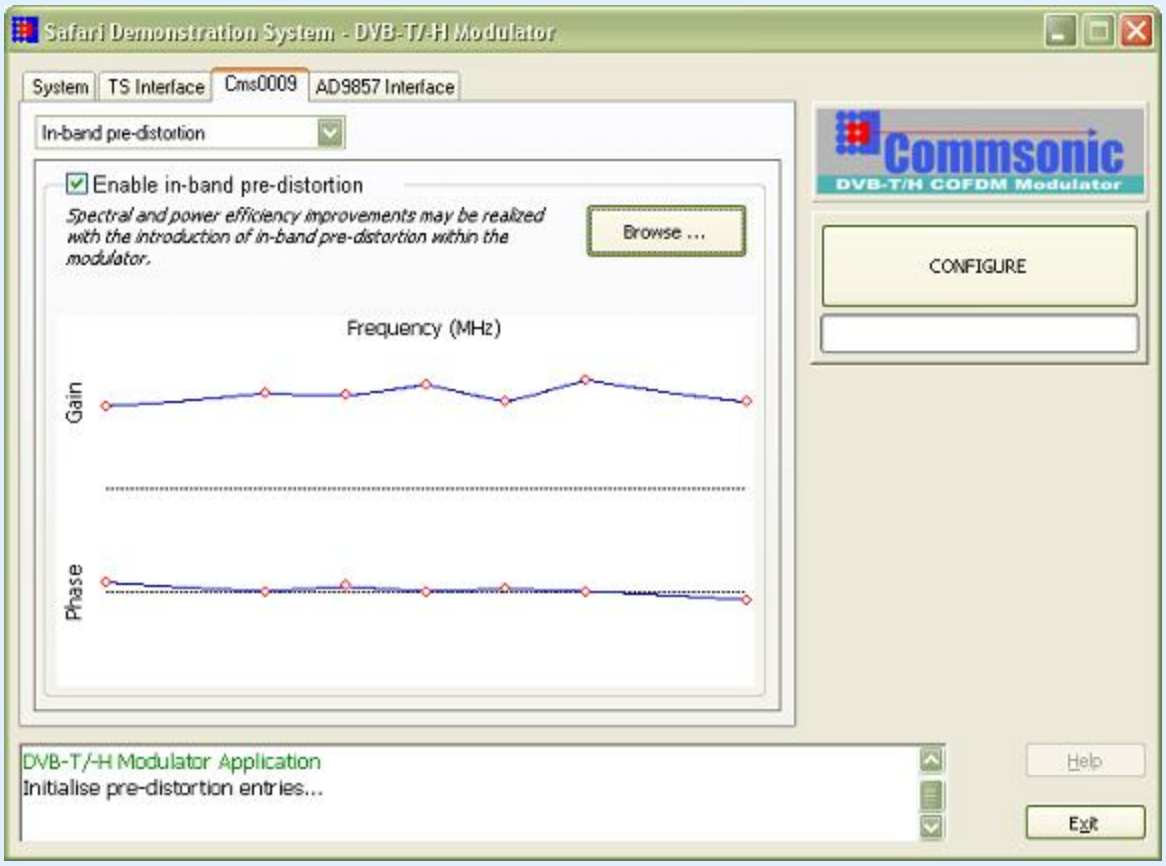
Up-sampled IFFT output using internal interpolation & up-conversion:

This application uses the DVB-T modulator core with internal interpolation that allows the channel bandwidth to be changed via a simple s/w register change. The DVB-T modulator internal up-conversion is also used which allows direct connection to external DAC devices

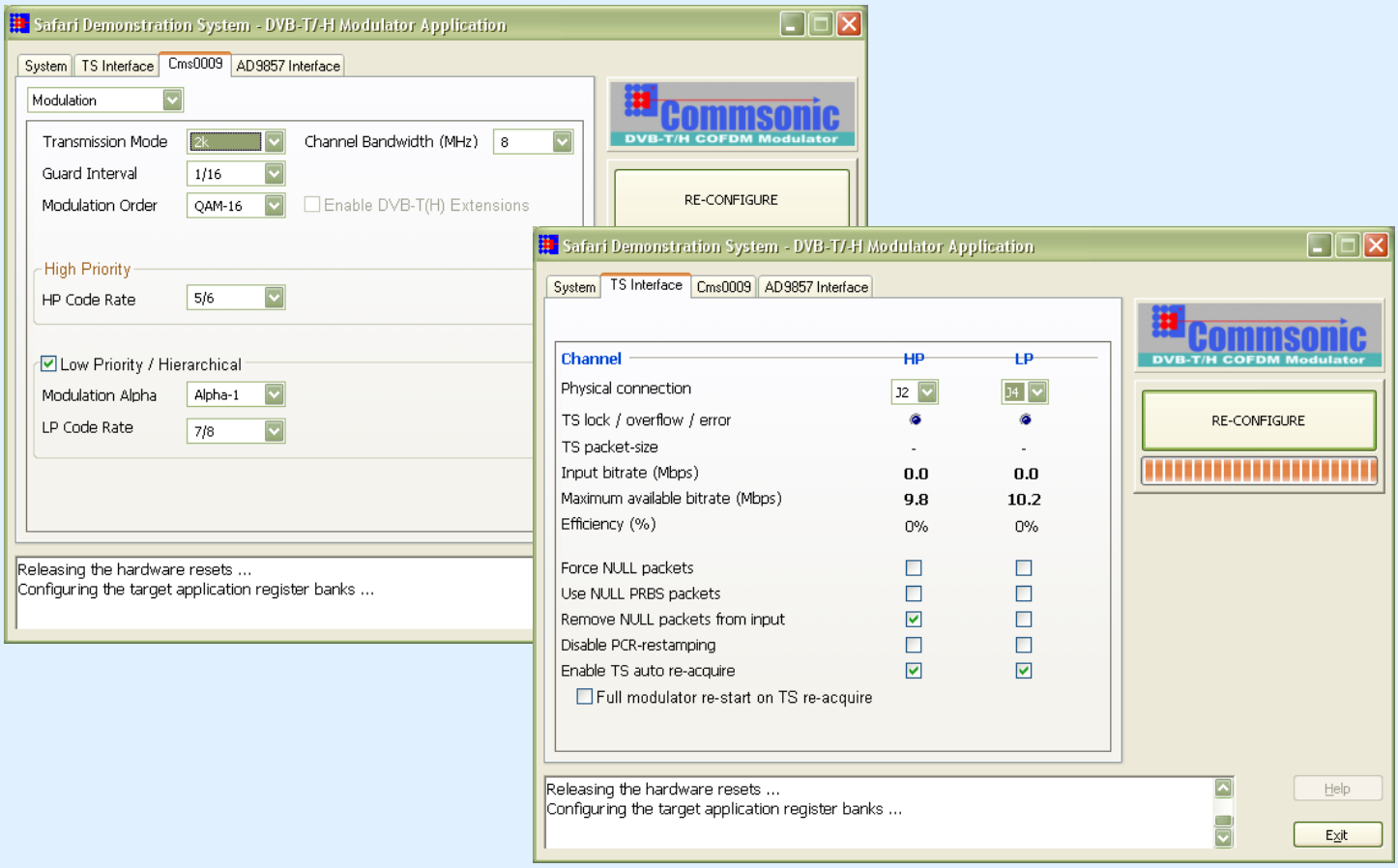


In-band pre-distortion

The core can be optionally configured to include an in-band pre-distortion module to compensate for group-delay distortion through the analog and RF amplifier stages.



Evaluation



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, ATSC-8VSB, ISDB-T, DVB-C/J.83/A/B/C, DVB-T/H and DVB-T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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