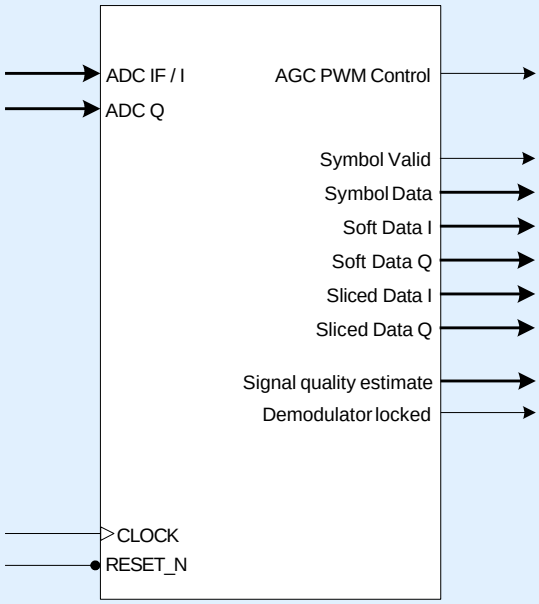
DVB-C/J.83 Cable Demodulator

CMS0022

- DVB-C EN 300 429
- ITU J83 Annexes A/B/C
- DOCSIS 1.1 / 2.0
- IF sub-sampling or I/Q baseband interface.
- Standard 188-byte MPEG Transport Stream output.
- Variable ADC width support.
- Single external clock source required.
- Single external analogue loop for AGC.
- Fully digital and automatic timing & frequency recovery - no VCXO or AFC required.
- Fully-digital matched channel filter for robust performance in the presence of ACI.
- Automatic QAM mode, FEC and spectral inversion searching.
- Pre-Viterbi and Pre-RS bit-error-rate (BER) statistics.
- Post-FEC bit-error-rate (BER) statistics.
- Blind and decision-directed adaption algorithms ensure rapid convergence of AGC, PLL and equaliser sub-systems.
- Automatic channel equalisation using LTE and DFE algorithms - signal quality estimate available.
- Symbol rate recovery up to approximately 40% of the master clock frequency.
- Full DVB-C/J83 QAM support: 16, 32, 64, 128, 256
- Implementation loss of <1dB for 128 or 256-QAM, and <0.5dB for other supported QAM modes.
- External RAM interface for long interleave modes.
- Number of debug signals available - carrier, timing lock, frequency offset etc.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).



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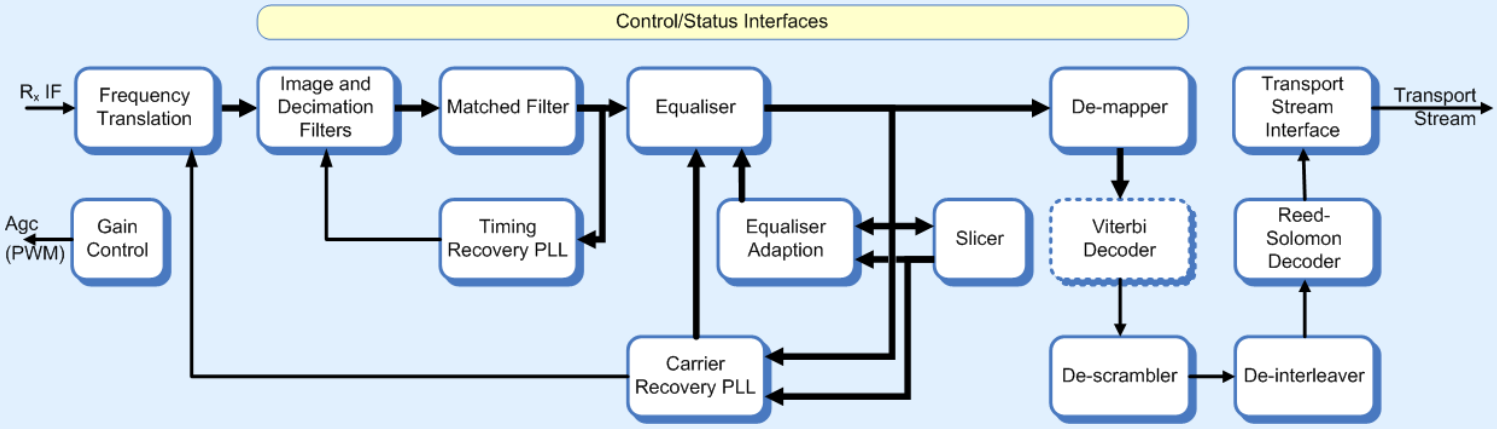
Block Diagram



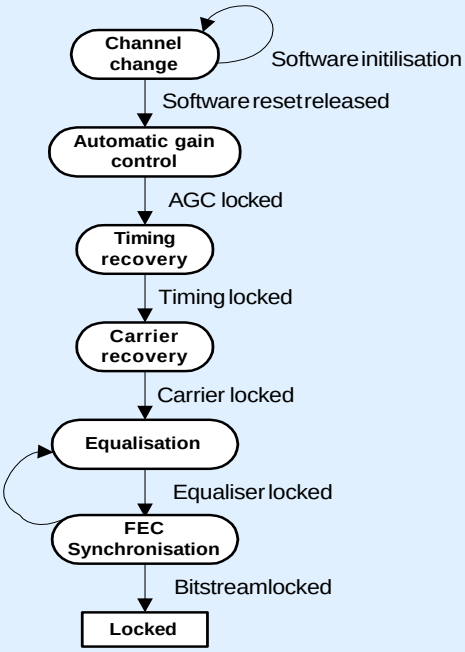
Detailed Description

The Commsonic CMS0022 DVB-C/J.83 Cable Demodulator is a 4th generation design that exploits Commsonic's experience of QAM and OFDM systems for broadband terrestrial, satellite and cable modems.

The core forms an integrated cable demodulator solution comprising of the Commsonic Universal QAM Demodulator(CMS0006) and J.83abc/DVB-C Cable FEC Decoder(CMS0018) cores.

The core has been designed to lock robustly in the presence of noise, frequency & timing offsets, static & dynamic multi-path channels and various other forms of interference. The demodulator core consists of four major sub-modules: the Radio interface & decimator, Symbol timing recovery, Equaliser and the FEC Decoder.

The operation of the demodulator is fully automated by an internal state machine.



Detailed Description (Cont'd)

A description of the processing steps follows:

Radio interface and decimator

The radio interface and decimator (RID) module is responsible for generating down-converted and filtered samples of the QAM input signal by performing external (analogue) gain control; IF mixing and image & decimation filtering.

ADC IF / I. The I component (or IF sub-sample) of the QAM input signal sampled at the input CLOCK rate. The format is configurable between 2's complement and offset binary.

ADC Q. The Q component of the QAM input signal sampled at the input CLOCK rate. The format is configurable between 2's complement and offset binary. Not used when IF sub-sampling is used.

AGC PWM control. A PWM control signal output to increase/decrease the gain of an external VGA. This allows the radio interface to control the level of the signal at the ADC input(s) to minimise the distortion due to clipping or quantisation.

Symbol timing recovery

The symbol timing recovery (STR) module is responsible for generating correctly timing constellation samples of the baseband & filtered signal by performing channel filtering; symbol rate detection and timing recovery.

Equaliser

The equaliser (EQU) module is responsible for generating the original QAM constellation by performing carrier frequency recovery; channel acquisition, equalisation & tracking and DC offset correction.

The equaliser provides a signal quality estimate calculated from the demodulated constellation noise. The estimate is available either from a software register or as signal output.

FEC Decoder

The FEC Decoder module combines all of the channel coding and Forward Error Correction functions specified by DVB-C and by J83 - Annexes A B and C. These include functions for QAM constellation slicing, trellis decoding, de-framing, de-scrambling, de-interleaving, and Reed-Solomon decoding.

The module provides automatic MPEG TS packet acquisition, including phase, bit, frame and byte alignment.

The module can be configured to generate Pre-Viterbi and Pre-RS bit-error-rate (BER) statistics.

Interleave memory may be configured for either on-chip or off-chip operation.

Synthesis Parameters

The CMS0022 core provides a number of synthesis options to allow the core to be optimised for its target application; for example, the length and structure of the equaliser can be tailored to suit the propagation conditions and may be omitted entirely where dispersion is not an issue.

Additionally unrequired cable standards may be omitted to minimise the size of the core.

The CMS0022 core may be optimised for either ASIC or FPGA synthesis to maximise the utilisation of the target architecture.

Register Configuration

The CMS0022 core is designed to acquire and lock to the input signal automatically with the external software application only specifying the input QAM order.

A number of expert registers are provided to allow the various control loop bandwidths and gains to be tweaked to ensure successfully demodulation even in the severest of environments.

Principle I/O Description

Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0022 register bank.
reg_wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
ADC Interface	
ADC IF / I	IF data (or I data) sampled at CLOCK rate. Format is configurable between 2's complement and offset binary.
ADC Q	Q data sampled at CLOCK rate (not used when IF sampling is used). Format is configurable between 2's complement and offset binary.
AGC PWM Control	AGC pulse width modulated output for signal level control at the ADC input(s).
Transport Stream Output	
ts_out_data	Decoded Transport Stream data bytes
ts_out_valid	1 => decoded data and sync outputs are valid
ts_out_sync	1 => current output byte is first in TS packet (0x47)
ts_out_next_rdy	1 => Next block in decoder chain is ready for new TS data byte. Data transfer occurs when ts_out_next_rdy = ts_out_valid = 1
External Memory Interface	
dtl_ram_addr	16-bit ram address
dtl_wr_ena	Active high RAM write enable
dtl_wr_data	8-bit RAM write data
dtl_rd_data	8-bit RAM read data
FEC Status	
vtr_phase_lock	AnnexB only : Indicates Viterbi decoder lock, the first stage of FEC acquisition
fec_sync_detect	AnnexB : Indicates detection of the FEC frame sync DVB-C : Indicates MPEG framing detection
mpeg_sync_detect	Indicates MPEG framing detection
rs_corrected_packet	RS decoder has corrected some errors in the most recent packet.
rs_uncorrectable	RS decoder has detected an uncorrectable packet
bitsync_locked	Overall status bit indicating the FEC is maintaining sync with the data stream
Others	
clock	Clock input – should be at least 2·5 x the bandwidth occupied by the modulation.
reset_n	Asynchronous active-low reset input.

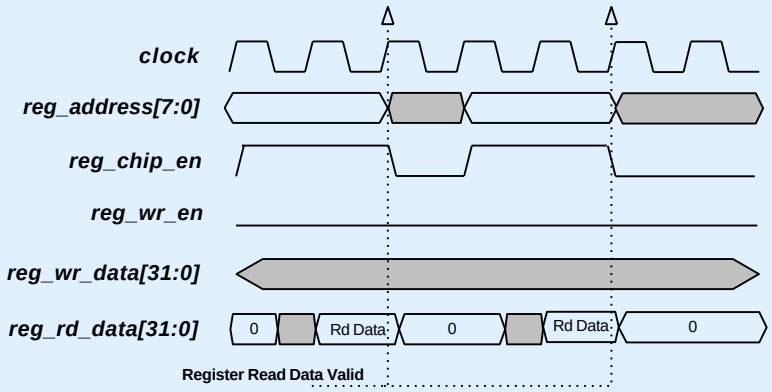
Register Interface

A simple 32-bit register-programming interface is provided. The register core can interface easily with whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

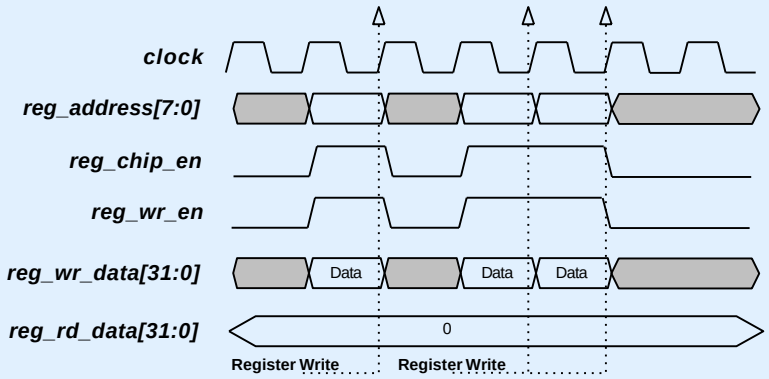
In addition to the mode control settings, the Register Interface also provides access to various system monitor registers including synchronisation status and BER measurement logic.

An active-high interrupt line is also available.

Register read access:

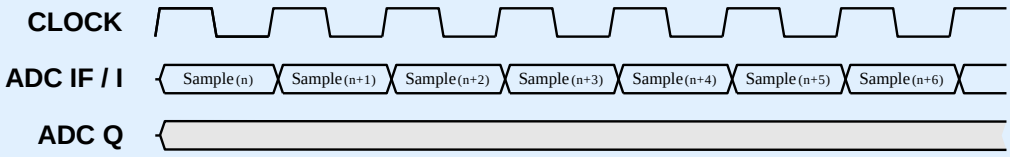


Register write access:

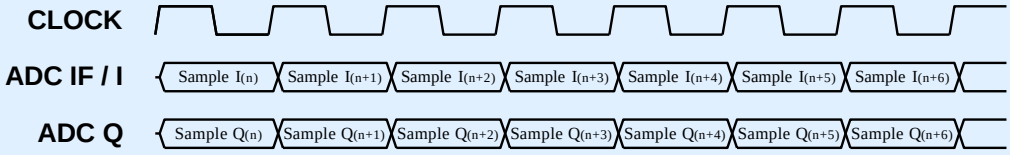


Timing Diagrams

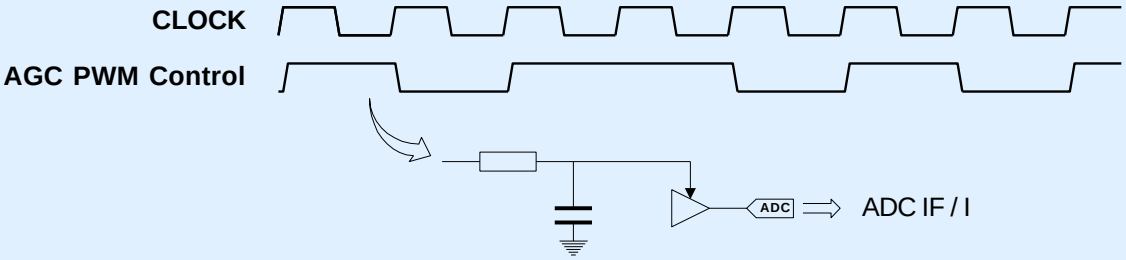
ADC IF Interface:



ADC I/Q Interface:

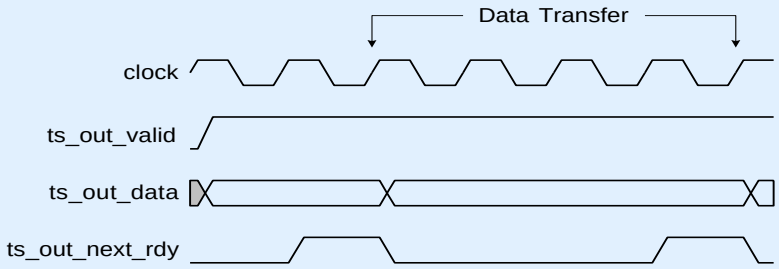


External Gain Control:



Timing Diagrams (Cont'd)

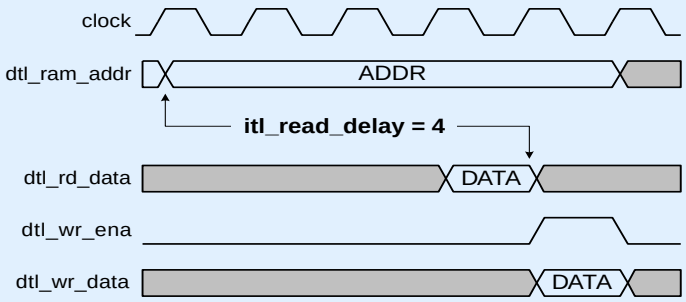
Transport Stream Output:



The output data interface is implemented with RDY-VALID handshaking. This provides a simple interface in which each block may moderate the data flow to match its own data processing requirements. The data source asserts its VALID flag when it presents data. The data destination indicates availability using its RDY flag. Data transfer occurs synchronously when both the source's VALID and the destination's RDY = 1.

External Memory Interface:

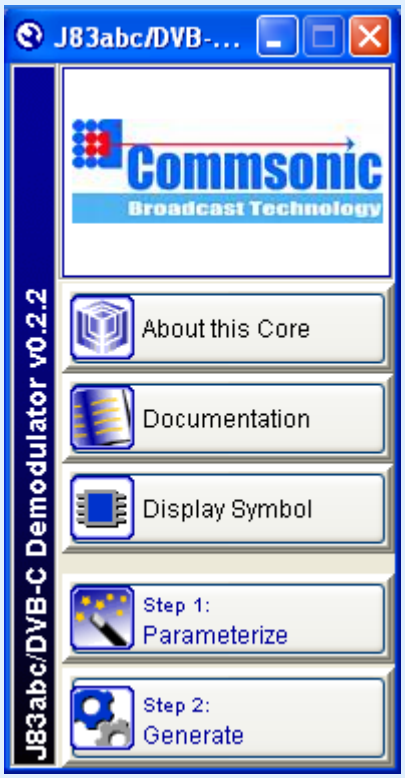
The CMS0022 may be configured to use memory external to the core. The timing of this interface is controlled by the synthesis constant **`itl_read_delay`**, illustrated below.



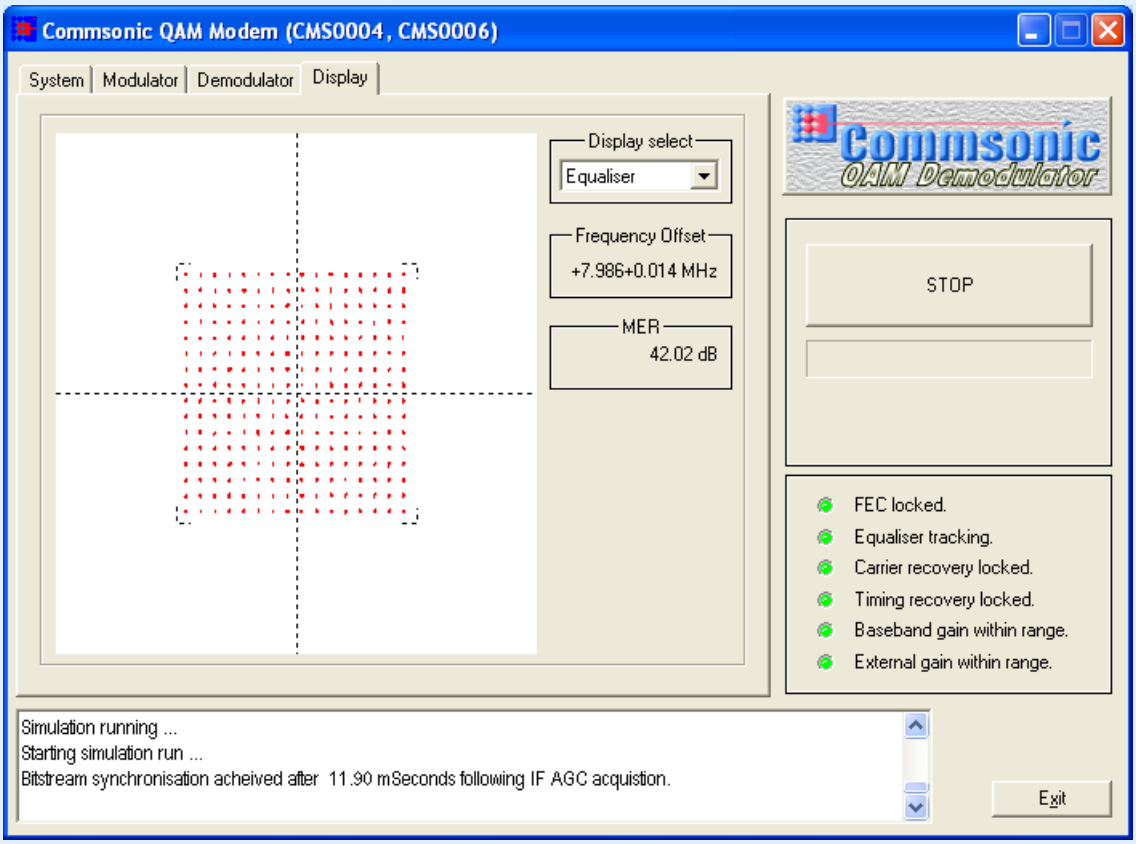
Altera® Megacore®

AMPP℠ Approved | OpenCore® Support | Qsys Compliant

The DVB-C/J.83 Cable Demodulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.



EVALUATION



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, ATSC-8VSB, DVB-C/J.83/A/B/C, DVB-T/H, DVB-T2 and ISDB-T.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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