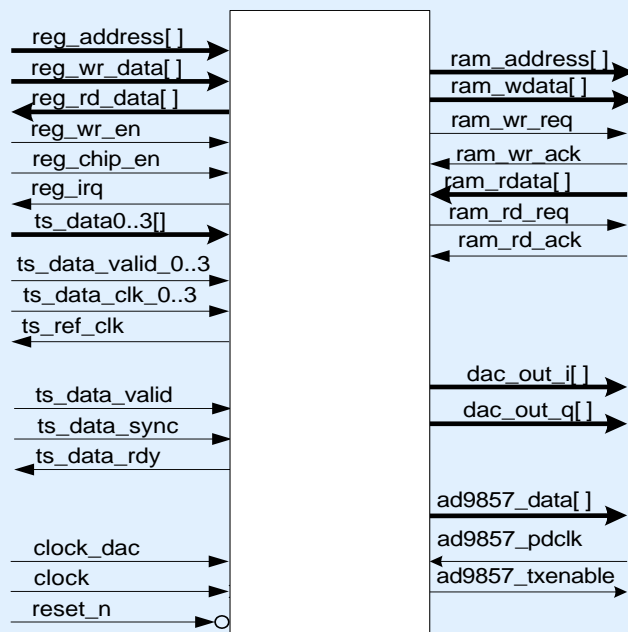


- Compliant with DVB-C (EN 300 429); ITU J.83 Annexes A, B and C; DOCSIS 1.x, 2.0 and 3.0.
- Scalable architecture supports 1 to 4 channels per core, and multiple instances per FPGA.
- Modulation accuracy > 45dB (MER).
- On-chip or off-chip interleaving RAM.
- Variable symbol-rate interpolation.
- Software selectable channel filter.
- AD9857/AD9957/AD9789 interface and auto-programming support.
- AD9516/ADF4350 PLL programming support.
- Extension core available for SPI/ASI interface with integrated PCR TS re-stamping, NULL TS packet removal/filtering and NULL/PRBS TS packet insertion.
- Seamless integration with Altera ASI megacore when using SPI/ASI extension core.
- Optional input and output TS rate estimation registers.
- Optional noise interference source
- Modes that are not required may be removed with synthesis options to generate a compact, efficient design.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures such as Altera® HardCopy.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).

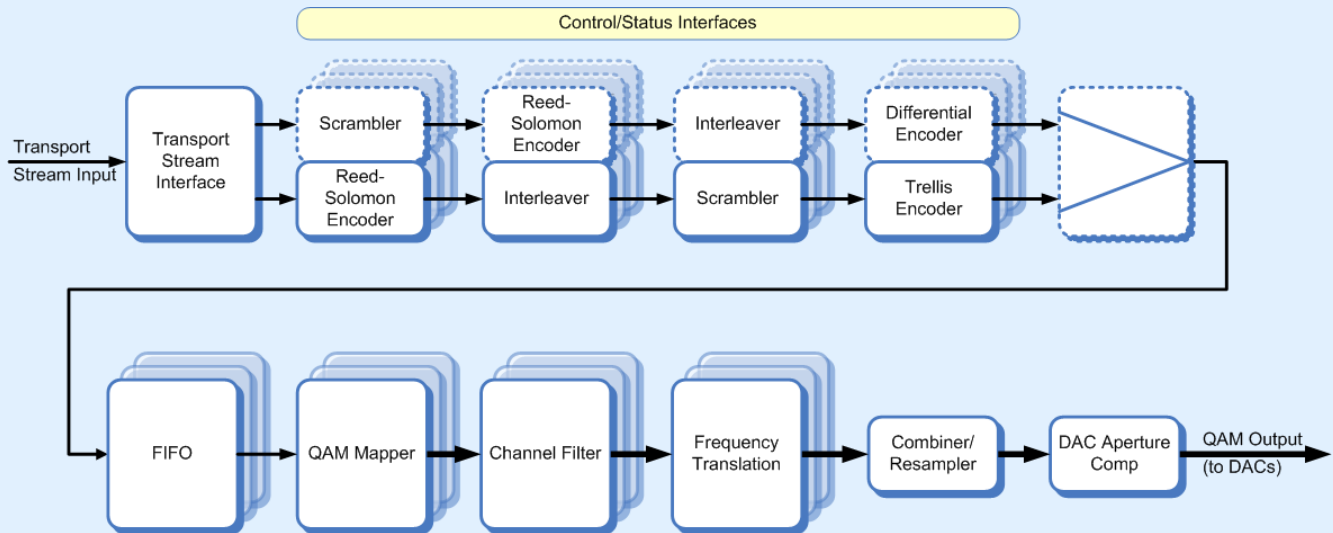


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## Block Diagram



## Detailed Description

The Commsonic CMS0024 Multi-channel Cable Modulator encodes up to four separate transport streams for J83 or DVB-C. The resulting QAM-symbols are filtered and up-converted, each channel to its own frequency division multiplex (FDM) sub-channel. The IF channels are then combined output to the radio interface as a single I/Q sample stream for translation to the final RF frequency.

Although most designs will implement only one of the cable standards, it is possible to synthesise the core to support any combination of standards in a single device.

Multiple instances of CMS0024 may be used on an FPGA, sharing access to a single external RAM device. This would typically take the form of a fast SRAM (or possibly SDRAM through a suitable SDRAM controller).

Multi-core implementations typically employ separate DACs for each core with the resulting modulated baseband or IF carriers up-converted to the assigned RF frequency bands and combined to produce the wideband cable transmission signal.

A description of the processing steps follows:

**Forward Error Correction.** The FEC is split into an 8-bit datapath for Annex A / C / DVB-C and a second 7-bit datapath for Annex B. The requirements differ to an extent that only the interleaver may be shared between them.

**FEC: J.83 Annex A + C and DVB-C.** The FEC requirements of J83 Annex A, Annex C and DVB-C are all identical except for supported QAM sizes and the channel filter roll-off parameter  $\alpha$ .

This is a relatively simple FEC, using a scrambler to randomise the data stream for good spectral characteristics, a Reed-Solomon code allowing correction of up to eight byte errors per MPEG packet, and a convolutional interleaver to disperse burst errors over multiple RS codewords.

**FEC: J.83 Annex B.** The FEC Annex B requires a more complex FEC. In addition to the techniques of scrambling, Reed-Solomon and interleaving used in Annex A, Annex B also includes a trellis code that complements the error-correcting capabilities of the RS code.

**FIFO.** The QAM Modulator accepts the formatted input streams from the FEC stage multiplexed over a time-division-multiplex (TDM) bus.

**Mapper.** The data passes through a FIFO into the mapper that selects the appropriate QAM mapping and constellation point.

**Channel Filter.** The selected constellation point is up-sampled and shaped/interpolated by a root-raised cosine FIR filter that can be programmed for the different transition factors (alphas) as required by the supported cable standards.

## Detailed Description (Cont'd)

A resampling interpolation stage provides complex baseband I/Q samples at the desired DAC clock frequency which would normally be a factor of at least  $4 \times N$  times the highest symbol rate to be supported, where N is number of channels.

**Frequency Translation.** Each modulated channel output signal is up-converted to low IF frequencies and combined to form a cluster of FDM channels. Typically the channels would be arranged on

## Operation

For single (multi-channel) instances of the CMS0024, all channels must have the same symbol rate and QAM mapping scheme. However varying interleaving depths can be supported. If mixed-mode operation is required then this can be arranged by instantiating multiple CMS0024 cores each with its own configuration of symbol rate and QAM scheme.

The CMS0024 core provides software register settings that are common for all channels within the core, e.g. FEC mode and symbol rate.

Further software registers are provided to define the spacing of FDM channels at the modulator output,

adjacent FDM channels spaced around DC by 6MHz (J.83) or 8MHz (DVB-C).

**DAC Aperture Comp.** The FDM output further processed to provide a composite signal to drive compatible DAC devices. The CMS0024 can provide parallel complex I/Q signals to input to a pair of DACs, or an interpolating DAC device such as the AD9857, AD9957 or AD9789. Optionally the output can be selected as an IF to supply a single DAC.

with the channels normally positioned symmetrically about DC (0Hz) to drive an I/Q RF modulator. It is also possible to modulate the FDM channels onto a low IF for use with a single DAC and superhet radio architectures that accept a real IF.

When multiple cores are implemented within a single FPGA then each core may be configured independently. This, for example, allows systems to transmit high-order QAM in the more reliable portions of the RF band while simultaneously transmitting low-order QAM on the less reliable frequencies.

## Principle I/O Description

<b>Register Bus Interface</b>	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0024 register bank.
reg_wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
<b>Transport Stream Interface</b>	
ts_data_0..3	8-bit Transport Stream data input (up to 4 ports/channels).
ts_data_valid	Transport Stream data valid input.
ts_data_sync	Transport Stream data sync input.
ts_data_rdy	Transport Stream path is ready for new byte. Data transferred when Ready and Valid are asserted together.
ts_data_refclk	Transport Stream reference clock output.
ts_data_clk_0..3	Transport Stream clock input (up to 4 ports/channels).
ts_data_valid_0..3	Transport Stream data valid input (up to 4 ports/channels).
<b>Interleaver external RAM Interface</b>	
ram_addr[]	Active RAM read/write address output from interleaver (external RAM option)
ram_wdata[]	Non-interleaved data output to RAM
ram_rdata[]	Interleaved data input from RAM
ram_rd_req	RAM read request output
ram_wr_req	RAM write request output
ram_rd_ack	RAM read acknowledge input
ram_wr_ack	RAM write acknowledge input
<b>Modulator Output Interface</b>	
dac_out_i	14-bit Transmit I complex output or IF output in IF mode.
dac_out_q	14-bit Transmit Q complex output.
ad9857_txdata	14-bit multiplexed data to the AD9857 if used.
ad9857_txenable	Controls the interface timing to the AD9857 if used.

**Principle I/O Description (Cont'd)**

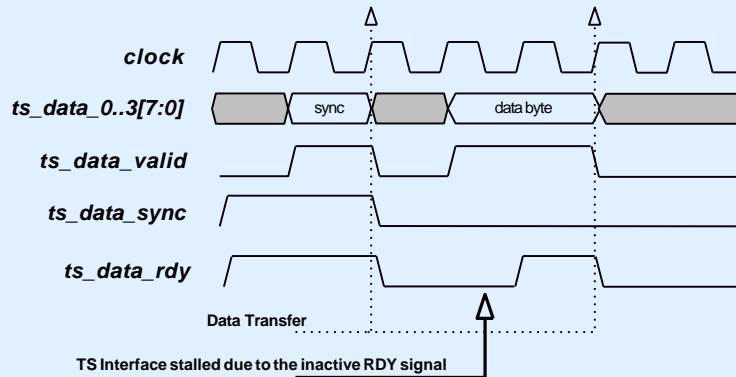
<b>Others</b>	
clock	Clock input.
ad9857_pdclk	AD9857 Clock.
reset_n	Asynchronous active-low reset input.

## Transport Stream Interface

### Standard TS interface:

The standard TS interface supplied uses a ready/valid handshake mechanism to allow data to be pulled through the modulator processing chain based on the on-air symbol rate. This requires the TS data source to be stalled when the modulator core is busy.

**Note**, the standard TS interface accepts TS data for **all** channels simultaneously. Consequently, the TS data on all channels must be synchronised – i.e. the 0x47 sync-bytes for all channels are transferred into the core on the same clock edge.



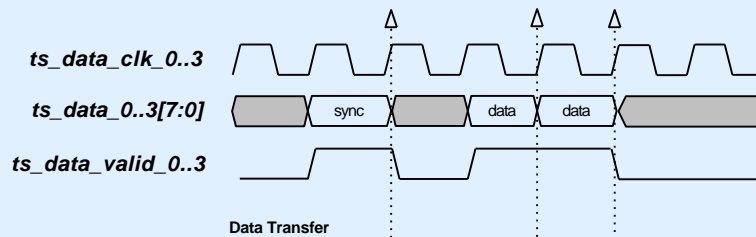
### PCR re-stamping TS interface:

In certain applications it may be that the input stream from the transport multiplexer is provided at a fixed rate and will not support the standard TS interface handshake mechanism and consequently some form of rate adaption is required. The TS PCR restamping extension core provides a simpler TS interface (compatible with SPI or ASI) to allow data to be input at any rate.

The core will be pad the input TS stream with NULL TS packets as required and perform any PCR adjustment.

When the PCR restamping extension core is used, an output signal, *ts\_data\_refclk* is provided that indicates the necessary 188-byte TS byterate to satisfy the on-air requirements.

**Note**, the PCR re-stamping TS interface accepts TS data for each channel independently. Consequently, the TS data on all channels does **not** need to be synchronised – i.e. the 0x47 sync-bytes for each channel may be transferred into the core on differing clock-edges. Furthermore, the *ts\_data\_clk* clock signal for each channel may be asynchronous to the *ts\_data\_clk* clock signal for other channels.



## Memory Requirements

Mode	RAM (kBytes) per Channel
J83 a/c DVB-C	2.4
J83b (short) DOCSIS 1.1/2.0	8
J83b (extended) DOCSIS 3.0	64

The principle use of RAM within the core is for the FEC interleaving function.

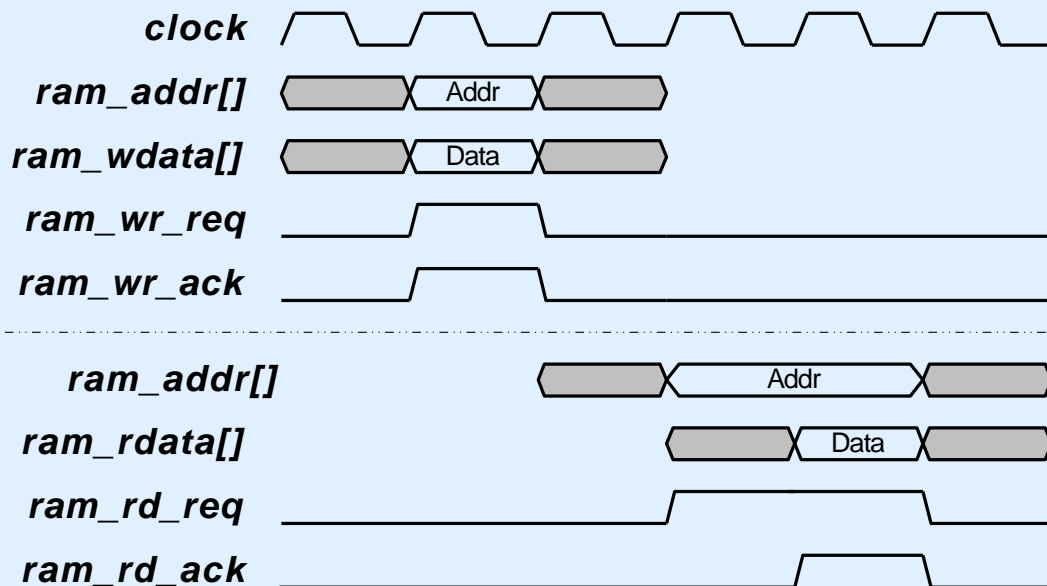
Internal FPGA memory is adequate for many applications, but prohibitive for the extended Annex B interleaving modes particularly for multi-channel configurations where the use of external RAM can lead to a significant reduction in system cost.

### Internal RAM

The Internal RAM uses FPGA SRAM. Bytes from each channel (1-4) are presented in parallel to the RAM as a single multi-byte word. Multiple cores may time-share a single RAM using a fixed access sequence, or *round-robin* polling. Up to 24 channels of Annex A or eight channels of Annex B (DOCSIS 1.1/2.0) may be implemented using a single 64kbyte MRAM found on the Altera Stratix devices.

### External RAM

The External RAM interleaver implements an arbitrated-burst RAM interface. This allows several cores to share a single off-chip SRAM or SDRAM (using a suitable controller).



## Clock Requirements

### Modulation

The primary clock-rate requirement for the core is a minimum 4 system-clocks per symbol per channel.

A typical 4-channel (7Msps) DVB-C core would require a master clock in excess of:

$$4 \times 4(\text{channels}) \times 7(\text{Max symbol-rate}) = 112\text{MHz.}$$

For this example, the single-sided occupied bandwidth at the DAC output would then be 16MHz (4 channels centred at -12, -4, +4 and +12 MHz).

Similarly, to provide 4 channels of J83B (5.35Msps) 256QAM requires a master clock frequency in excess of 86MHz.

### DAC output interface

The DAC output interface normally operates at the master clock frequency (e.g. 112MHz for 4-channel DVB-C), but may be configured to operate at a lower rate when driving the AD9857 DDS/DAC (which is unable to directly support the max sample rate provided by the 4-channel core).

### Shared RAM

The SRAM interleaver can share SRAM among several CMS0024 cores using a simple access sequencer/scheduler. Each CMS0024 core presents multi-byte parallel data to the SRAM.

**Annex A with SRAM:** Each core requires RAM access for four clocks per symbol. Hence, six four-channel cores – providing 24 DVB-C channels – may share a single MRAM with 24 clocks per symbol.

**Annex B (short) with SRAM:** The SRAM interleaver processes 7-bit galois symbols in 4 clocks. In 256-QAM mode,

$$\text{clocks\_per\_symbol} > \text{num\_cores} * 4 * 8/7$$

Two 4-channel cores may share one MRAM using much fewer than the 16 clocks per symbol required by the channel filter.

**Multi-channel RAM:** The clock requirement for external RAM access depends on the number of cores per RAM and the RAM access time.

$$\text{Minimum clocks rate} = \text{Core0\_symbol\_rate} * 4 + \text{Core1\_symbol\_rate} * 4 + \text{Core2\_symbol\_rate} * 4.$$



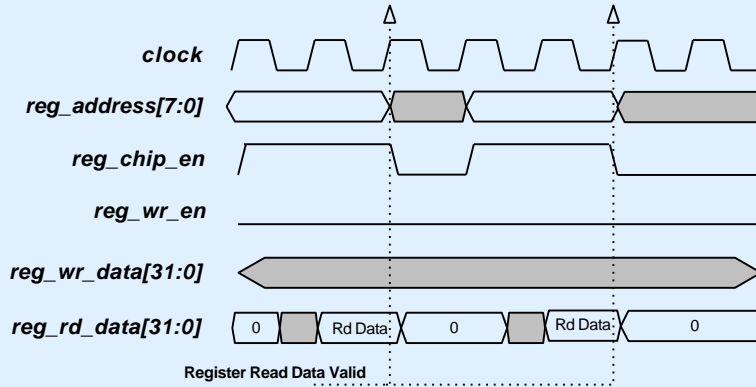
## Register Interface

A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I<sup>2</sup>C, 8-bit, big-endian, little-endian, etc). The register-core can be interface

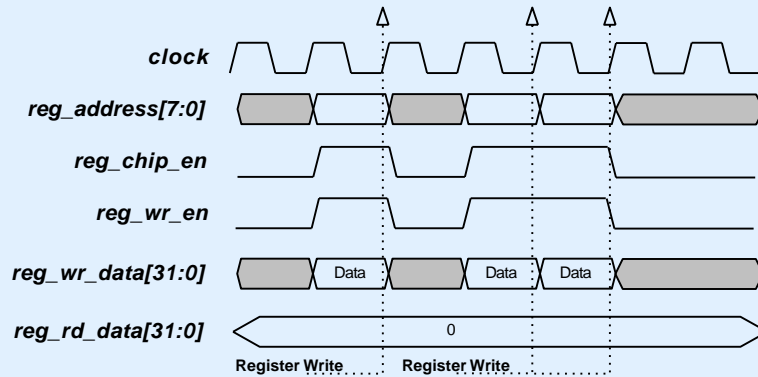
directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

An active-high interrupt line is also available.

### Register read access:



### Register write access:

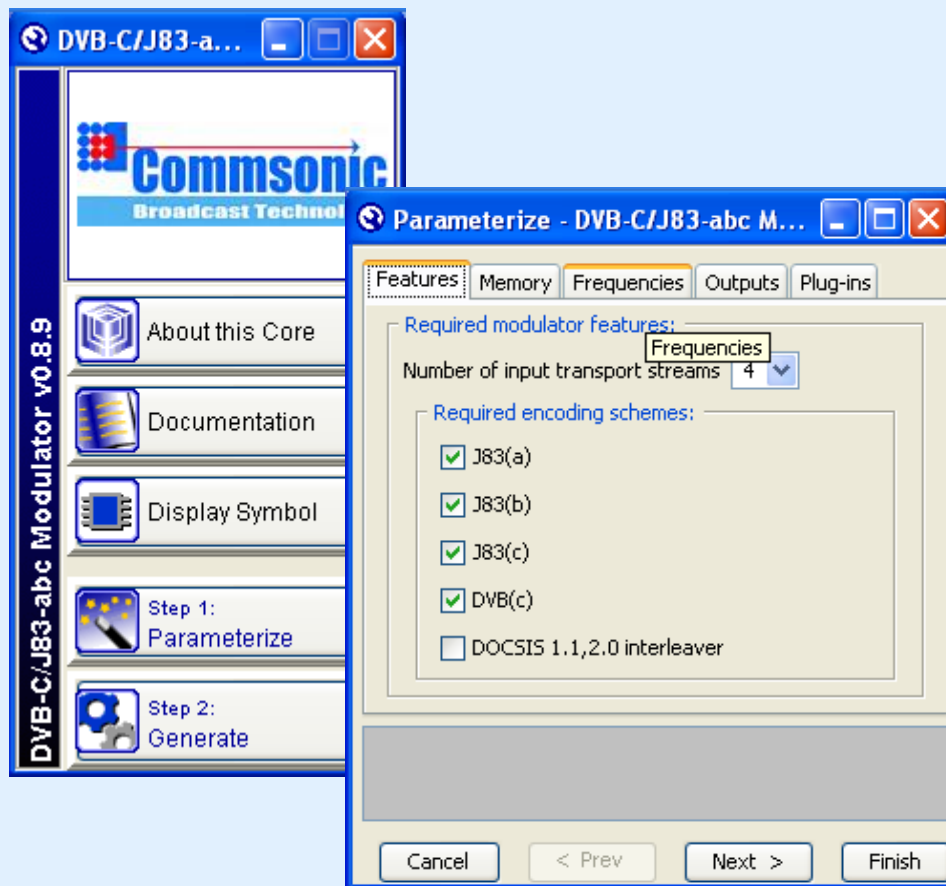


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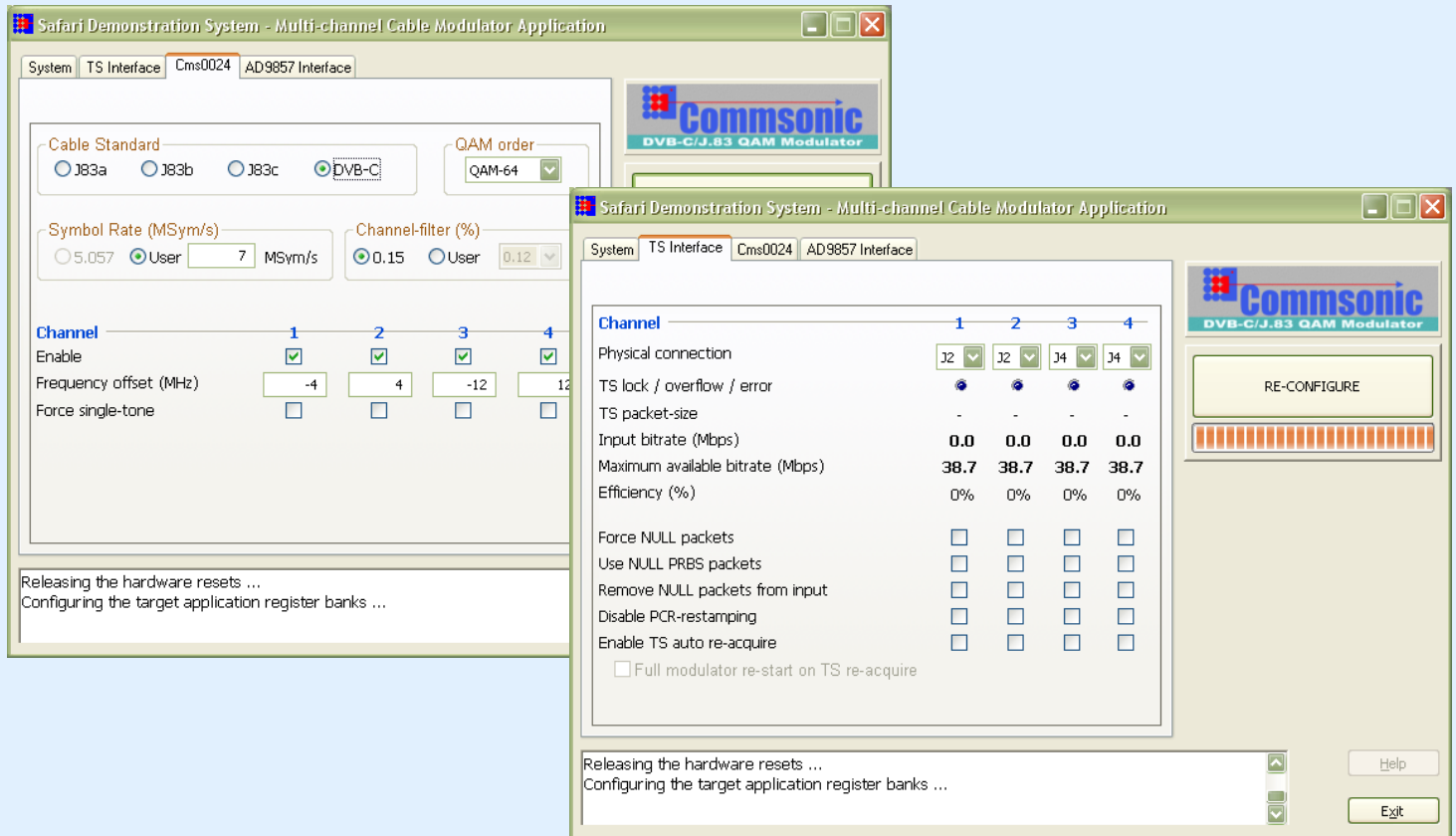


The Multi-channel Cable Modulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters

are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.



## EVALUATION



### About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, DVB-CID, ATSC-8VSB, ISDB-T, DVB-C/J.83/A/B/C, DVB-T/H and DVB-T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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