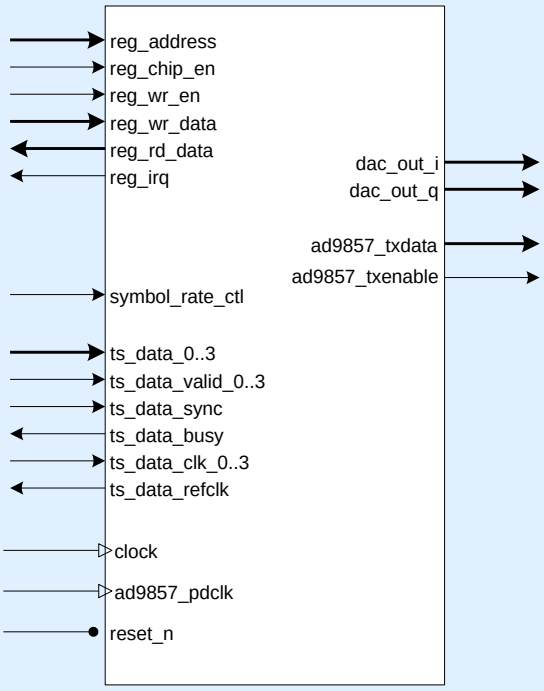
Multi-channel ATSC 8-VSB Modulator

CMS0038

- Compliant with ATSC A/53 8-VSB
- Scalable architecture supports 1 to 4 channels per core, and multiple instances per FPGA.
- Variable sample-rate interpolation provides ultra-flexible clocking strategy
- Integrated Reed Solomon/Convolutional channel coder
- Automatic insertion of Segment Sync, Field Sync and Pilot signals
- Extension core available for SPI/ASI interface with integrated PCR TS re-stamping.
- Extension core available for SMPTE 310M interface with DPLL timing synchronisation
- Flexible DAC interface compatible with baseband I/Q and IF DAC subsystems
- Optional interface to Analog Devices AD9857/AD9957 DDS DAC
- Modes that are not required may be removed with synthesis options to generate a compact, efficient design.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures.
- Supplied as a protected bitstream or netlist (Megacore® also available for Altera® targets).



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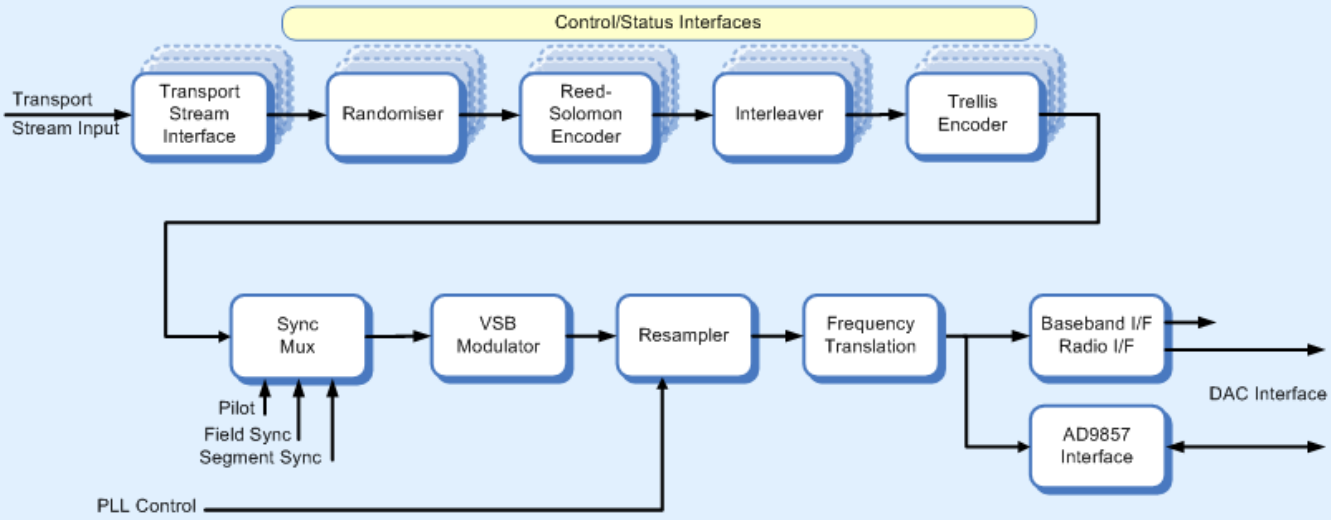
Block Diagram



Detailed Description

The Commsonic CMS0038 Multi-channel ATSC 8-VSB Modulator encodes up to four separate transport streams. With an integrated Channel Coder, the CMS0038 core has been designed specifically to implement the 8-VSB requirements of the ATSC Digital Television Standard (A/53).

The core provides all the necessary processing steps to modulate the transport streams into complex I/Q signal pairs for further filtering. Each channel is up converted to its own frequency division multiplex (FDM) sub-channel before being combined and input to a pair of DACs, or a DDS up-conversion DAC such as the AD9857(or AD9957). Optionally, the output can be selected as an IF to supply a single DAC.

Multi-core implementations typically employ separate DACs for each core with the resulting modulated baseband or IF carriers up-converted to the assigned RF frequency bands and combined to produce the wideband transmission signal.

The design has been optimised to provide excellent performance in FPGA devices.

A description of the processing steps follows:

Randomiser. This block performs energy dispersal by scrambling the incoming transport stream packets with a pseudo-random sequence.

Reed-Solomon Encoder. This block constructs 207-byte Reed Solomon codewords by applying a T=10 (207,187) code to the scrambled transport stream packets.

Interleaver. This block uses convolutional byte interleaving to disperse the Reed Solomon codewords over a period of approximately 4ms.

Convolutional Encoder. This block applies a rate 2/3 convolutional code to the interleaved data by means of a 4-state trellis encoder. The 3-bit encoder output symbols are mapped to 8-level 8-VSB constellation points.

Sync Multiplexer. This block inserts Field Sync and Segment Sync sequences into the transmitted symbol stream and adds a low-level Pilot signal. These signals are used for physical-layer synchronisation at the receiver.

VSB Modulation. This block performs vestigial sideband modulation of a locally-generated baseband carrier, driven by the composite output from the Sync Multiplexer.

Detailed Description (cont'd)

Rate Conversion. This block re-samples the complex samples output from the VSB Modulation block at symbol-rate into complex samples at a sub-multiple of the DAC/core clock frequency.

A frequency control input is provided to allow the modulation symbol rate to be locked to the data rate on the transport stream interface. This would typically be driven by a PLL, for example when the SMPTE 310M interface option is selected.

Baseband-to-IF. This block provides the option to mix the signal up to a higher IF as defined by a software register. The block may be removed using synthesis options if it is not required.

Radio Interface. This block performs some final, register-selectable processing functions to optimise the output for the radio in the target application. For example, the data can be formatted to work with either twos-complement or offset-binary DAC devices. In addition the data is formatted to suit the external device that could take separate I/Q, multiplexed I/Q or a single IF output.

Additional modes are provided to support the Analog Devices AD9857 device that provides up-conversion, SINC filtering and DAC functions in a single package. The AD9857 device requires that the I/Q data be multiplexed onto a single data bus. The *ad9857_pdclk* input is provided to enable this feature and should be sourced from the AD9857 PDCLK output

Control/Status Interface. The Control/Status interface is provided by a synchronous, 32-bit register bank. Full details of the registers within the modulator core are contained within the full data sheet.

Principle I/O Description

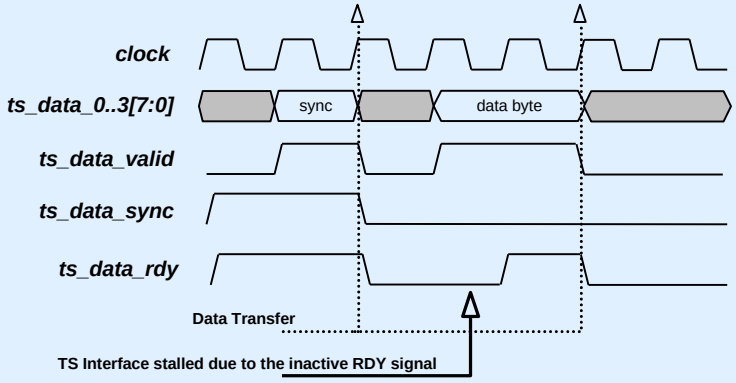
Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0038 register bank.
reg_wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
Transport Stream Interface	
ts_data_0..3	8-bit Transport Stream data input (up to 4 ports/channels).
ts_data_valid_0..3	Transport Stream data valid input (up to 4 ports/channels).
ts_data_sync	Transport Stream data sync input.
ts_data_busy	Transport Stream interface is busy. TS data should be stalled until the interface is available again.
ts_data_clk_0..3	Transport Stream clock input (up to 4 ports/channels).
ts_data_refclk	Transport Stream reference clock output.
Modulator Output Interface	
dac_out_i	14-bit Transmit I complex output or IF output in IF mode.
dac_out_q	14-bit Transmit Q complex output.
ad9857_txdata	14-bit multiplexed data to the AD9857 if used.
ad9857_txenable	Controls the interface timing to the AD9857 if used.
Others	
clock	Clock input at greater than 4x 8-VSB symbol-rate (> 43.049MHz).
ad9857_pdclk	AD9857 Clock.
Symbol_rate_ctl	Symbol rate frequency control input. This input would typically be driven from a PLL when the modulation rate must be locked to the data rate on the transport stream interface.
reset_n	Asynchronous active-low reset input.

Transport Stream (TS) Interface

Standard TS interface:

The standard TS interface supplied uses a ready/valid handshake mechanism to allow data to be pulled through the modulator processing chain based on the on-air symbol rate. This requires the TS data source to be stalled when the modulator core is busy.

Note, the standard TS interface accepts TS data for **all** channels simultaneously. Consequently, the TS data on all channels must be synchronised – i.e. the 0x47 sync-bytes for all channels are transferred into the core on the same clock edge.



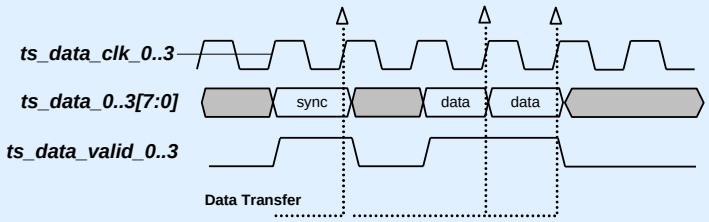
PCR re-stamping TS interface:

Typically the input stream from the transport multiplexer is provided at a fixed rate that requires 'padding' to match the required on-air bitrate; consequently some form of traditional MPEG TS rate adaption is required. The TS PCR restamping extension core provides a simpler TS interface (compatible with SPI or ASI) to allow data to be input at an asynchronous rate.

When the PCR restamping extension core is used, the core will pad the input TS stream with NULL TS packets as required and perform any PCR adjustment. An output signal, *ts_data_refclk* is provided that indicates the necessary 188-byte TS byte rate to satisfy the on-air requirements.

The core provides a symbol rate control input for applications that require a synchronous relationship between the modulation symbol rate and TS bit rate. This would normally be driven as part of a PLL controlling the fill state of an input TS FIFO.

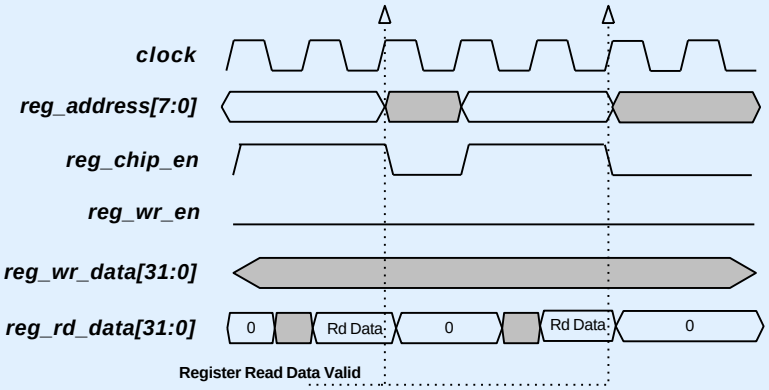
Note, the PCR re-stamping TS interface accepts TS data for each channel independently. Consequently, the TS data on all channels does **not** need to be synchronised – i.e. the 0x47 sync-bytes for each channel may be transferred into the core on differing clock-edges. Furthermore, the *ts_data_clk* clock signal for each channel may be asynchronous to the *ts_data_clk* clock signal for other channels.



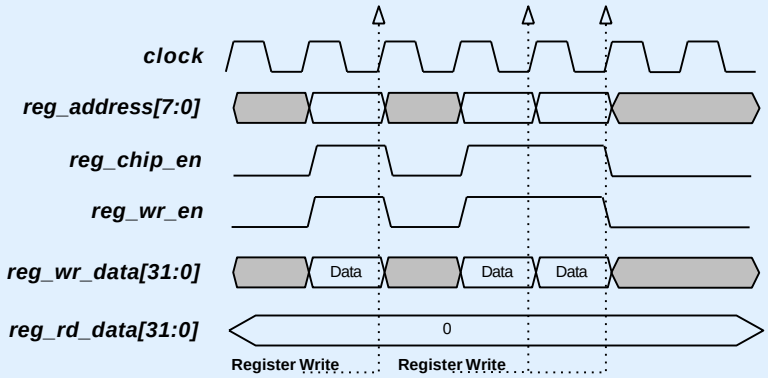
Register Interface

A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

Register read access:



Register write access:

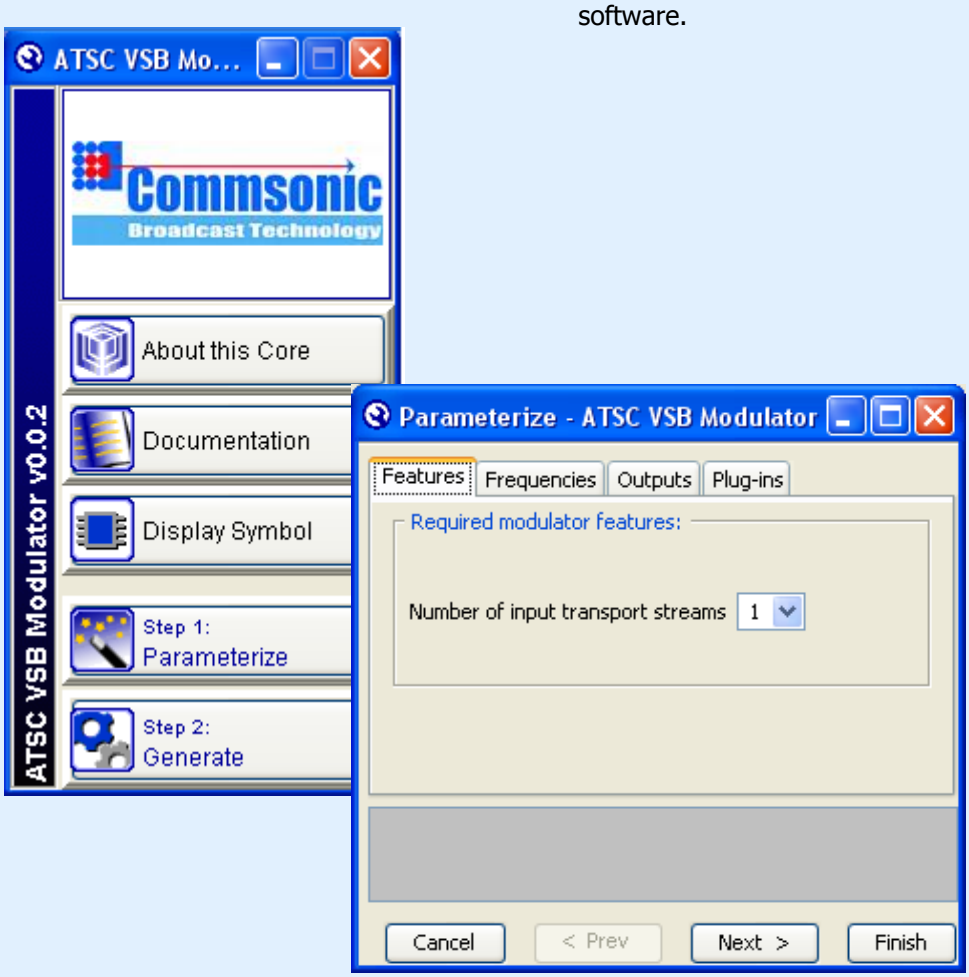


Altera® Megacore®

OpenCore® Support

Qsys Compliant

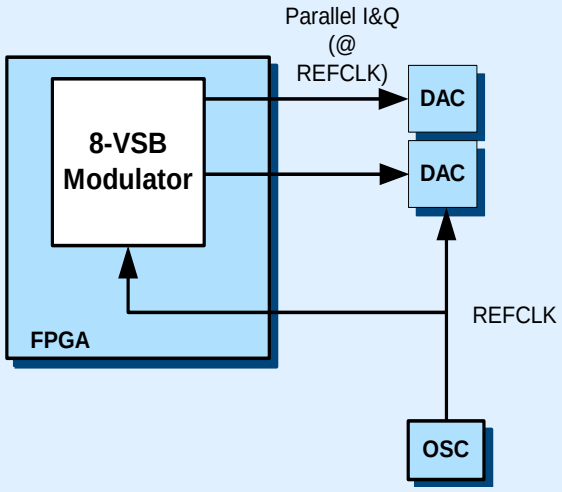
The Multi-channel ATSC 8-VSB Modulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.



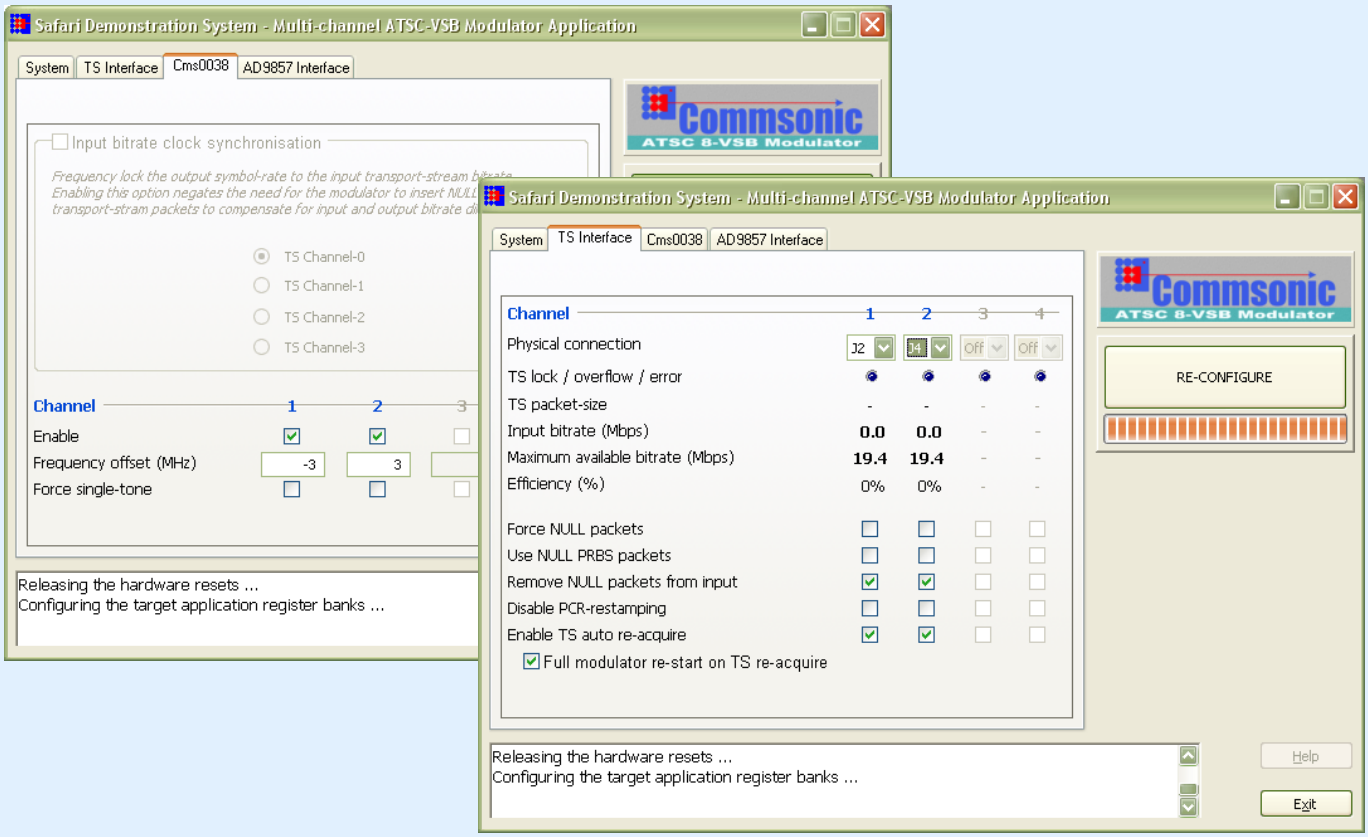
EXAMPLE APPLICATIONS

Up-sampled output using internal interpolation & up-conversion:

This application uses the CMS0038 with internal interpolation and direct baseband I/Q interfacing to external DACs.



EVALUATION



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, ATSC-8VSB, DVB-C/J.83/A/B/C, DVB-T/H, DVB-T2 and ISDB-T.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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