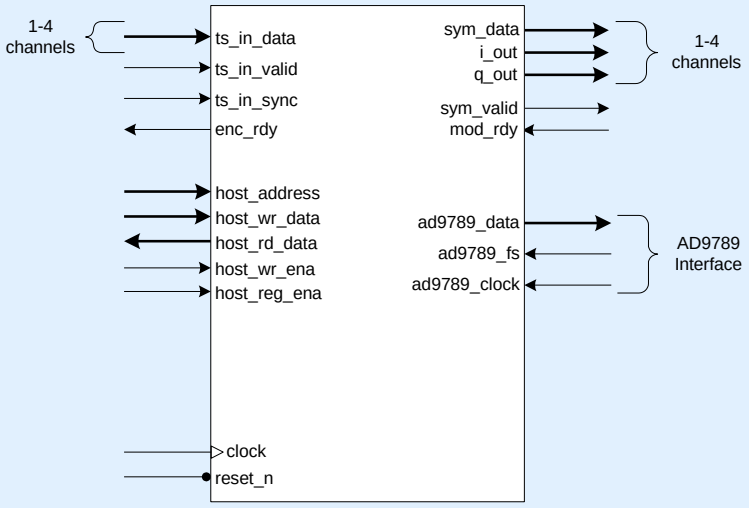
Multi-Channel J.83abc/DVB-C Cable FEC Encoder

CMS0044

- Provides a multi-channel FEC encoding solution for cable transmission compliant with DVB-C (EN 300 429); ITU J.83ABC; DOCSIS 1.0-3.0 and SCTE 07.
- Scalable architecture supports 1 to 4 channels per core, and multiple instances per FPGA.
- Mapped and unmapped symbol data outputs
- Supports AD9789 Signal-Processing DAC.
- 4-channel cores may be cascaded, allowing multiple cores to arbitrate into a single external SRAM.
- Extension core available for SPI/ASI interface with integrated PCR TS re-stamping, NULL TS packet removal/filtering and NULL/PRBS TS packet insertion. TS interface accepts 188- or 204-byte MPEG packets
- Seamless integration with Altera ASI megacore when using SPI/ASI extension core.
- Optional input and output TS rate estimation registers.
- Synthesis control to build for any subset of the supported modes, minimizing logic.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures such as Altera® HardCopy.
- C / C++ header file defines Host Interface registers, facilitating software mode control.



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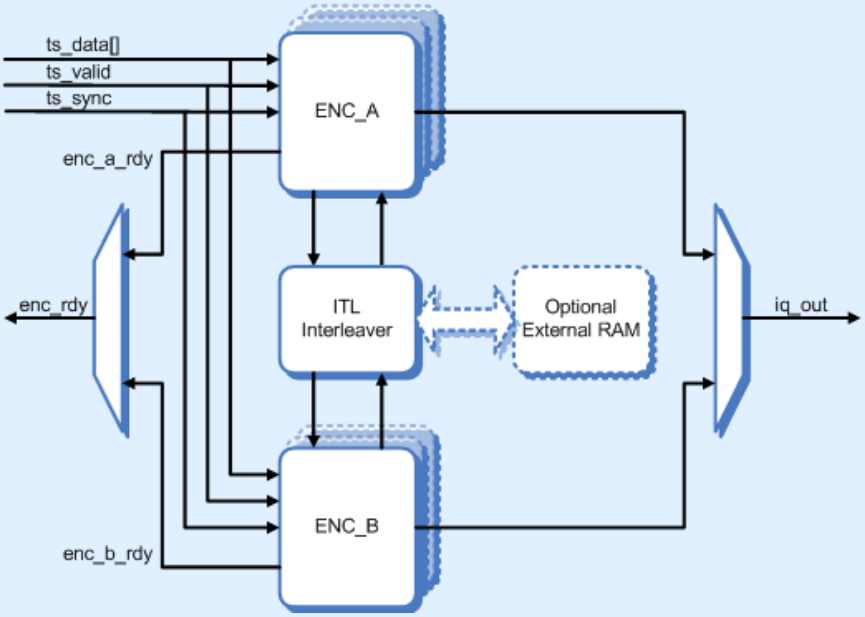
Block Diagram



Detailed Description

The Commsonic CMS0044 J.83abc/DVB-C Cable FEC Encoder combines all of the channel coding and Forward Error Correction functions specified by DVB-C and by J83 Annexes A B and C. It is designed to interface to external modulators or advanced upconverting DACs such as the Analog Devices AD9789.

The CMS0044 includes functions for framing, scrambling, interleaving, Reed-Solomon coding, trellis coding, and QAM mapping.

The requirements of J83A J83C and DVB-C are virtually identical, but are quite different to the requirements for J83B. With the exception of the common interleaver block, two independent datapaths are required, as shown above.

The multi-channel encoder uses a common transmission mode, so symbol timing is common for all channels. The encoder may be built with individual interleave modes, as this does not impact data symbol timing. However, this requires more memory bandwidth.

ENC_A (DVB-C and J.83 Annex A + C)

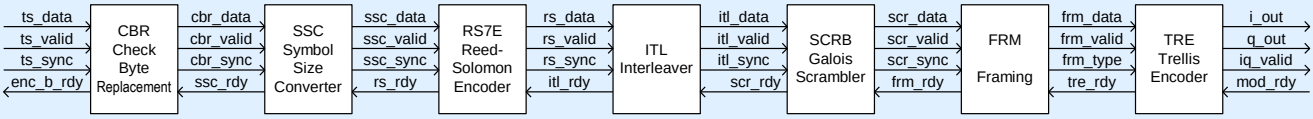
The ENC_A sub-block supports the full set of DVBC constellations, of which J.83 Annex A and C are subsets. This includes 16-, 32-, 64-, 128- and 256-QAM.

These modes use a single interleave configuration.

Mode control is provided via the host interface registers. Annex A/C-mode is selected by setting the ***AnnexBEnable*** register = 0.

The number of bits per symbol is set by ***QamMode*** = bits_per_symbol – 4

ENC_B (J.83 Annex B)



The ENC_B sub-block supports J.83 Annex B.

CBR replaces the 0x47 MPEG sync byte with a checksum, used in the decoder both as a method of sync detection and to monitor the decoded transport stream for errors.

SSC converts the 8-bit Transport Stream bytes into 7-bit data symbols for the Reed-Solomon Encoder. The 7-bit RS(128,122) code contains one extension symbol.

The Interleaver supports the full set of J.83 B modes, but there are synthesis options for shorter modes specified for DOCSIS and SCTE07, reducing memory requirements by up to a factor of eight.

The scrambler is based on a second-order Galois polynomial using the same 7-bit Galois Field as the Reed-Solomon Encoder.

The Framer block synchronises the Scrambler and the Trellis Encoder to the RS packet boundaries. A fixed sync pattern is followed by a four-bit field specifying the Interleave mode to be used by the decoder.

Mode control is provided via the host interface registers. Annex B mode is selected by setting the ***AnnexBEnable*** register = 1.

The number of bits per symbol is set by ***QamMode*** = bits_per_symbol – 4.

The 4-bit ***ItlMode*** is encoded as specified in J.83 Annex B.

Synthesis Parameters

Build parameters are defined in a VHDL package and applied to the design as GENERICs.

These are fixed at synthesis time.

Name	Description	Default
build_num_chan	Number of channels	4
build_j83_a	Selects whether to build support for J.83 Annex A	TRUE
build_j83_b	Selects whether to build support for J.83 Annex B	TRUE
build_j83_c	Selects whether to build support for J.83 Annex C	TRUE
build_dvb_c	Selects whether to build support for DVB-C	TRUE
build_external_itl_ram	Selects whether to build the external RAM interface (TRUE) or instantiate internal RAM (FALSE).	FALSE
build_docsis_itl	If true, only shorter Annex B interleave modes are built in accordance with DOCSIS 1.0 and 1.1. (Note DOCSIS 2.0 and 3.0 specify the full range of Annex B modes. The parameter name is kept for historical reasons.)	FALSE
docsis_itl_size_128x	This parameter is only used if build_docsis_itl = TRUE. In addition to supporting the 128x1 max interleave specified by DOCISIS 1.0/1.1, it also provides support for the 128x4 maximum size specified by SCTE 07. It also allows non-standard applications to reduce memory usage by reducing the maximum interleave. For a value N in the range 1-7, the maximum interleave supported is 128xN.	1
build_common_itl	If true, a common interleave mode is used for all channels. If false, each channel has independent interleave mode control. All other mode controls are common between channels.	TRUE
host_addr_width	Width of the host address bus	6
host_data_width	Width of the host data bus	32

Principle I/O Description

Transport Stream Inputs	
ts_in_data	Uncoded data input bytes (1-4 channels)
ts_in_valid	1 => uncoded data and sync inputs are valid
ts_in_sync	1 => current input byte is first in TS packet (0x47)
enc_rdy	Output : 1 => Encoder ready for new data byte. Data transfer occurs when enc_rdy = ts_in_valid = 1
Symbol Data Outputs	
sym_data	The unmapped data output symbols (1-4 channels)
sym_valid	Indicates current output symbol is valid (mapped and / or unmapped)
i_out	This 5-bit signed output represents the in-phase portion of the mapped symbol
q_out	This 5-bit signed output represents the quadrature portion of the mapped symbol
mod_rdy	Handshaking input which signals transfer of symbol data to modulator. Symbol data (sym_data / i_out / q_out) transfer occurs when mod_rdy = sym_valid = 1 This signal is unused when configured with AD9789 Plug-in
ad9789_data	AD9789 symbol data – connect to AD9789 Data Bus
ad9789_fs	AD9789 symbol rate – connect to AD9789 FS Pin
ad9789_clock	AD9789 Input clock – connect to AD9789 clock
External Memory Interface	
itl_ram_addr	16-bit RAM address
itl_wr_data	Nx8-bit RAM write data
itl_wr_req	Active high RAM write request output
itl_wr_ack	Active high RAM write acknowledge input
itl_rd_data	Nx8-bit RAM read data
itl_rd_req	Active high RAM read request output
itl_rd_ack	Active high RAM read acknowledge input
Others	
clock	Clock Input.
reset_n	Asynchronous reset input (active low).

Host Interface	
host_addr	6-bit register address
host_reg_ena	Active high enable (chip select) Must be high for read or write access.
host_wr_data	32-bit register write data (only 16 bits used)
host_wr_ena	1 => write cycle ena (write data valid)
host_reg_ena	1 => active register access (read or write).
host_rd_data	32-bit register read data (only 16 bits used)

Host Interface Registers

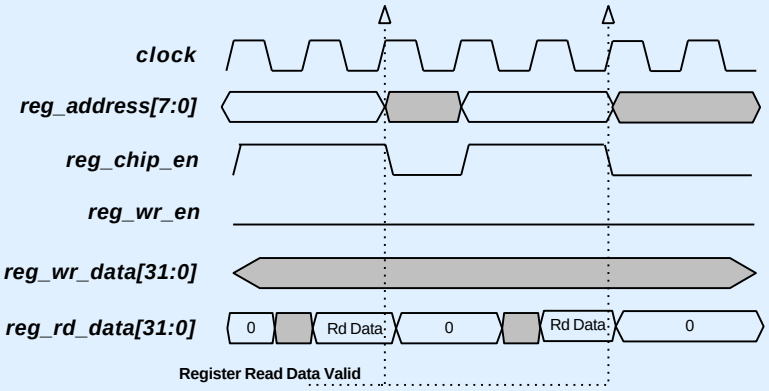
A simple 32-bit register-programming interface is provided. The host interface registers allow software to control the encoder's mode of operation. The register core interfaces easily to the host interface format appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

For programming convenience, the CMS0044 package includes a standard C / C++ header file defining the host register bank as a structure. The members of that structure are as follows:

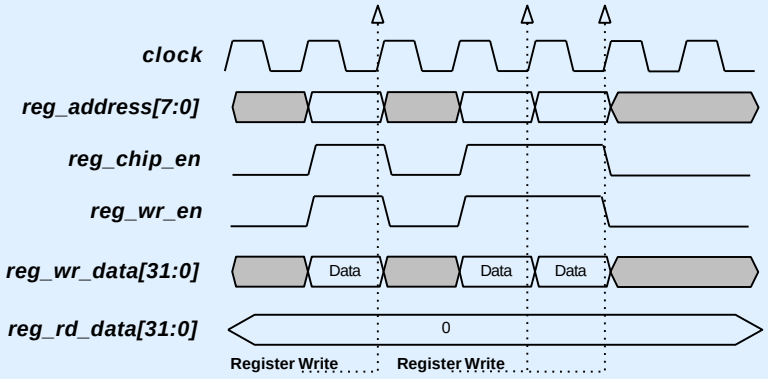
Name	Address	Description
SoftReset	0x00	Write 1 to this register to force all internal states to reset. Remaining register contents are unaffected. This register dafults to 1 on hardware reset, so a zero must be written here to enable the core.
Version	0x04	This read-only register returns the version number of the core.
AnnexBEnable	0x08	1 => Annex B mode. 0 => Annex A+C+DVBC
QamMode	0x0C	Specifies the number of bits per symbol : QamMode = bits_per_symbol – 4
ItlMode	0x10	When in Annex B mode, this register specifies the Interleave mode. Encoding matches that of J.83 Annex B.

An active-high interrupt line is also available.

Register read timing :



Register write timing :



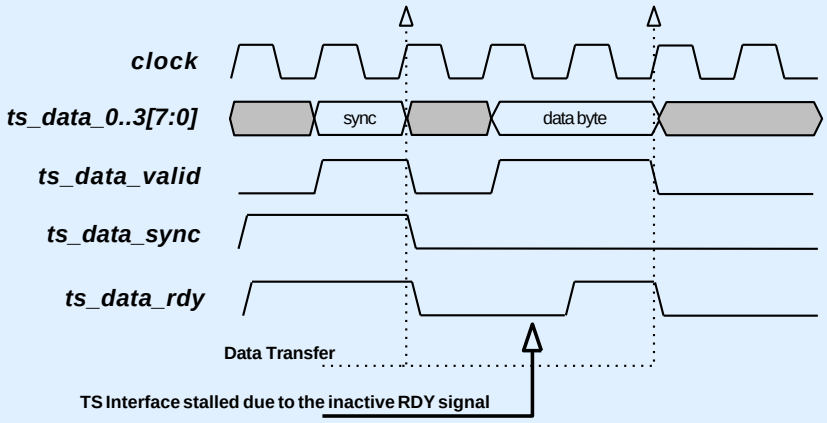
Data I/O

The standard input and output data interfaces are implemented with RDY-VALID handshaking. This provides a simple interface in which each block may moderate the data flow to match its own data processing requirements. The data source asserts its VALID flag when it presents data. The data destination indicates availability using its RDY flag. Data transfer occurs synchronously when both the source's VALID and the destination's RDY = 1.

Standard TS interface:

The standard TS interface supplied uses a ready/valid handshake mechanism. Data is pulled through the modulator processing chain based on the on-air symbol rate. The TS data source stalls its output flow when the core is busy.

Note, the standard TS interface accepts TS data for **all** channels simultaneously. Consequently, the TS data on all channels must be synchronised – i.e. the 0x47 sync-bytes for all channels are transferred into the core on the same clock edge.



Symbol-Locked TS Interface

Applications with local video encoders or TS packet re-timing can build the Symbol-Locked TS Interface. The CMS0044 provides a byte-rate reference clock *ts_data_refclk* locked to the symbol timing strobe.

The local TS source can use this signal for timing reference, providing data to the core at the exact required rate.

Notes The Symbol-Locked TS interface accepts TS data for all channels in parallel. TS data on all channels must be synchronised – the 0x47 sync-bytes for each channel must occur (along with ts_sync) on the same ts_valid cycle. *ts_data_clk_0* is used for all channels and may be asynchronous to the core clock. 188-byte packets are required.

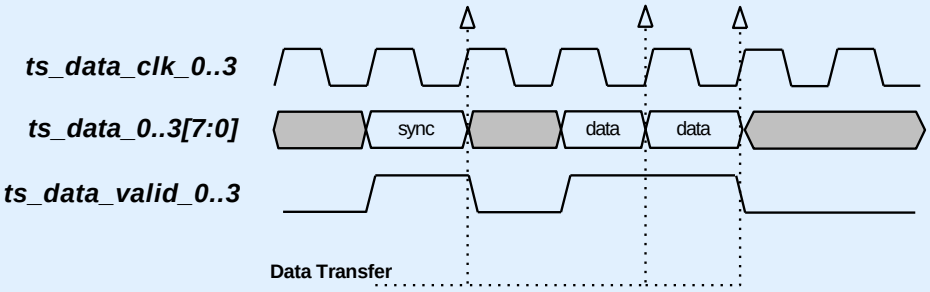
PCR re-stamping TS interface:

When the input Transport Stream is provided at a fixed rate which does not match the required on-air data rate, rate adaption is required. The TS PCR restamping extension core provides a simpler TS interface (compatible with SPI or ASI) to allow data to be input at any rate.

The core pads the input TS stream with NULL TS packets as required and performs the required PCR timestamp adjustment.

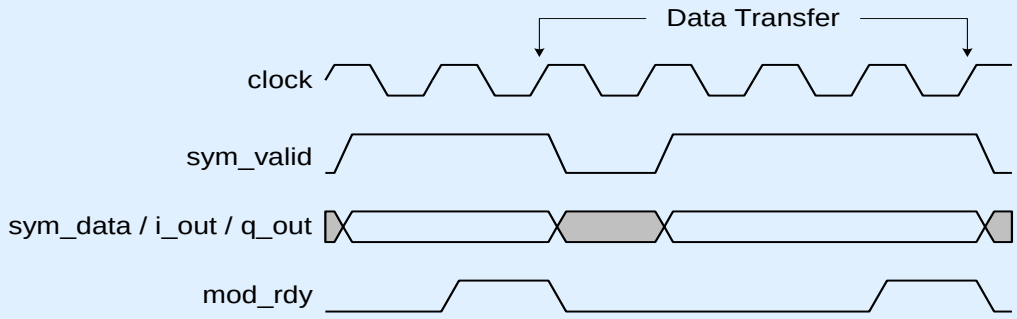
The PCR restamping extension core accepts either 188- or 204-byte packets. However, the *ts_data_refclk* output indicates only the required byte rate for 188-byte TS.

Notes The PCR re-stamping TS interface accepts TS data for each channel independently. Consequently, the TS data on all channels does **not** need to be synchronised. The 0x47 sync-bytes for each channel may be transferred into the core at different times. Furthermore, the *ts_data_clk* clock signal for each channel may be asynchronous to the *ts_data_clk* clock signal for other channels.



Symbol Output:

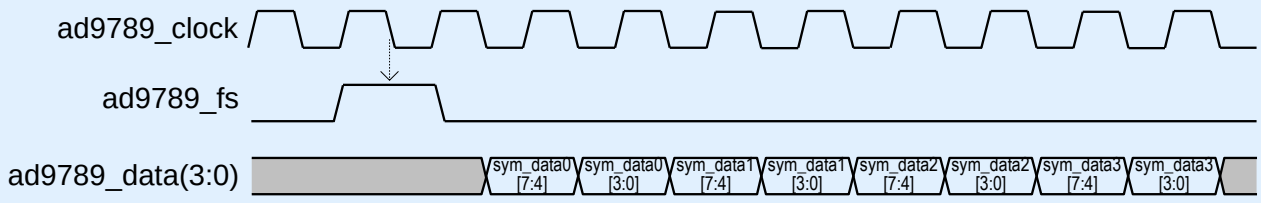
The basic symbol data interface includes mapped and unmapped data, regulated by a RDY-VALID handshake. All channels share common RDY_VALID handshake signals.



Interface for the AD9789 Modulator / DAC:

As an alternative to the basic symbol interface shown above, the CMS0044 also supports the Analog Devices™ AD9789. This advanced signal processing DAC provides 4-channel QAM modulation and upconversion capability. The CMS0044 provides 4-channels of FEC encoded data to the AD9789 using only a small number of FPGA pins. This functional density potentially allows a large number of cable channels using a single FEC FPGA.

Four channels of symbol data are transferred sequentially over the ad9789_data bus, which may be configured with 4, 8, 16 or 32-bit width. The example below illustrates transfer over a 4-bit bus. The CMS0044 data is timed from the falling edge of ad9789_clock.



Memory Requirements

The principle use of RAM within the core is for the interleaving function.

Internal FPGA memory is adequate for many applications, but prohibitive for the extended Annex B interleaving modes, particularly for multi-channel configurations where the use of external RAM can lead to a significant reduction in system cost.

Mode	RAM (kBytes) per Channel
J83 a/c DVB-C	2·4
J83b (short) DOCSIS 1.1/2.0	8
J83b (extended) DOCSIS 3.0	64

Internal RAM

When configured for internal RAM, FPGA SRAM is instantiated inside the CMS0044. When operating in Individual Interleave Mode (as in DOCSIS 3.0), the interleave data from each channel is presented to a different RAM. In Common Interleave Mode, the channel data bytes are catenated into a multi-byte parallel data word, applied to a single RAM.

External RAM

"External" RAM can be either on-chip or off-chip, but is external to the CMS0044 itself. RAM may be shared among several CMS0044 cores using a fixed access sequence, or *round-robin* polling. On-chip RAM provides dual-port access and processes one interleave word per clock. Off-chip SRAM typically has a single bidirectional data bus, requiring separate read and write cycles and additional bus turn-around cycles.

These examples assume Common Interleave Mode. Independent Interleave Mode requires four times the stated clock rate.

Annex A with On-chip M-RAM: Up to 16 four-channel cores, providing up to 64 DVB-C channels, may share a common Altera M-RAM using only a single clock per symbol per core.

Annex B with Off-Chip Synchronous SRAM: Because the interleaver processes 7-bit Galois symbols, more than one Interleave cycle may be required per symbol. It is also necessary to allow time for data bus turn-around.

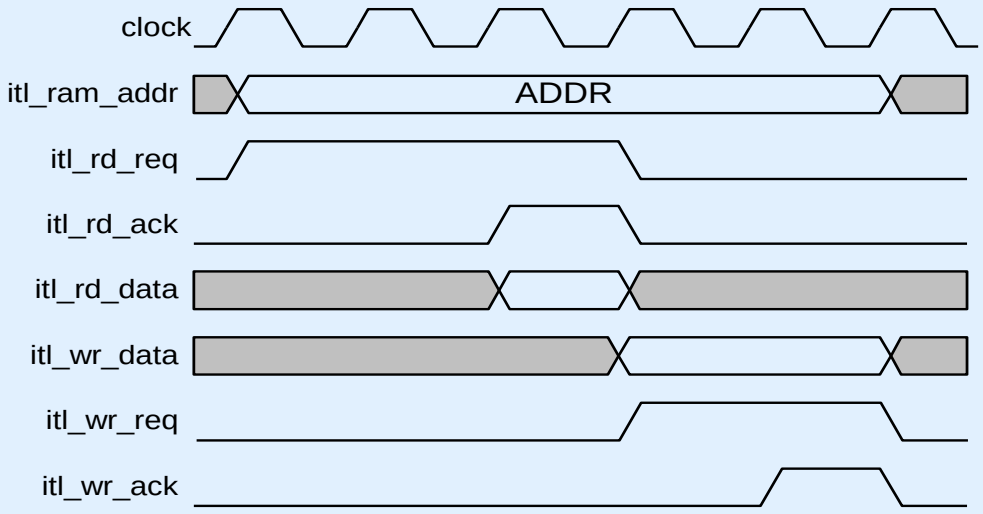
clocks/symbol = 2.2 x (number_of_cores + 1).

QDR SRAM: QDR SRAM has separate read and write busses and provides the same throughput as on-chip memory. Sixteen Annex B encoders (four 4-channel cores) can share a 1 MB QDR SRAM chip.

clocks/symbol = 1.1 x number_of_cores.

External Memory Interface Timing:

REQ-ACK handshaking allows multiple cores to arbitrate into a common external memory.



Plug-Ins and Expansions

The CMS0044 is designed for flexibility and expandability. Expansion kits allow several cms0044 cores to share a common external memory (standard or QDR SRAM).

Transport Stream interface Plug-ins provide support for ASI / SPI interfaces with rate adaption, Null stuffing and PCR correction. There is also a symbol-locked TS reference clock Plug-in, providing a byte-rate reference clock for local MPEG encoders.

About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, ATSC-8VSB, DVB-C/J.83/A/B/C, DVB-T/H, DVB-T2 and ISDB-T.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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