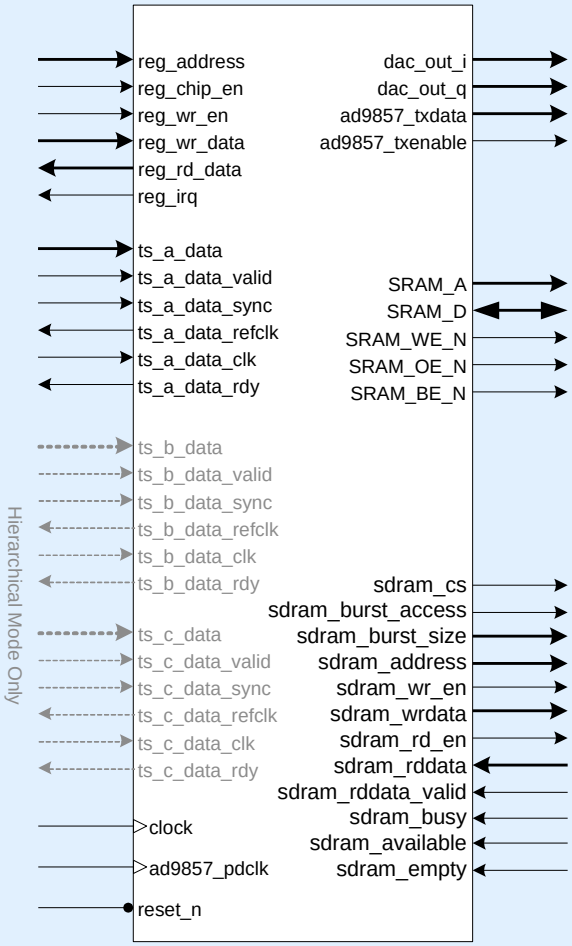
ISDB-T Modulator

CMS0045

- Fully compliant with both ARIB STD-B31 and ABNT NBR 15601
- Enables rapid development of audio/visual systems using commodity Free-to-Air set-top-box technology and low-cost FPGAs.
- Supports SDRAM or Synchronous SRAM
- 1-segment or 13-segment operation
- 2K, 4K and 8K OFDM modes
- Hierarchical transmission - Fully configurable for up to three layers, each independently configurable to carry one of the TS inputs.
- Variable channel bandwidth support using a single clock reference.
- Optional DAC interfaces support AD9857/9957/9789 with auto-programming interface.
- Optional FFT output windowing.
- Optional in-band equalizer.
- Optional CPU-free configuration.
- Optional auxiliary channel support.
- Optional critical filter for ">25Watt" mask.
- Dual-core combining for multi-channel applications.
- Extension core available for SPI/ASI interface with integrated PCR TS re-stamping, NULL TS packet removal/filtering, NULL/PRBS TS packet insertion, input and output TS rate estimation registers. Seamless integration with Altera ASI megacore.
- Extension core for BTS support.
- Extension core for SFN synchronisation.
- Synthesis options for reduced functionality allow a range of compact, efficient designs, some without external RAM.
- Designed for very efficient FPGA implementation without compromising ASIC deployment.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).



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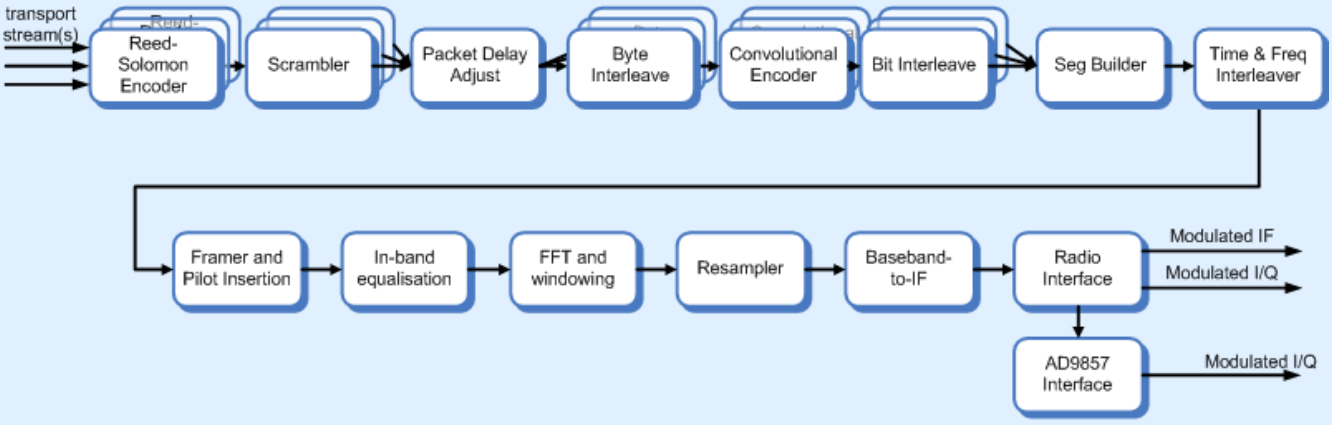
Block Diagram



Detailed Description

The Commsonic CMS0045 ISDB-T Modulator provides all the necessary processing steps to modulate one, two or three transport stream into a complex I/Q signal for input to a pair of DACs, or an interpolating DAC device such as the AD9857/9957 or AD9789. Optionally the output can be selected as an IF to supply a single DAC.

The design has been optimised to provide excellent performance in low cost FPGA devices such as the Cyclone™ range from Altera or the Spartan™ range from Xilinx

A description of the processing steps follows:

Reed-Solomon Encoder. This block generates Reed Solomon packets based on the industry standard MPEG RS(204, 188) code.

Scrambling. This block provides energy dispersal using the randomisation polynomial $1+x^{14}+x^{15}$.

Packet Delay Adjustment. Because the different Hierarchical Layers have different delays through the Byte Interleavers, each Layer is delayed to ensure the total delay through the system is an integer number of frames.

Byte Interleaver. This block performs the outer interleaving function with depth I=12 as specified by the ISDB-T standard.

Convolutional Encoder. This block performs convolutional encoding and data-rate puncturing.

Bit Interleaver. This provides additional time-dispersal of the signal for improved rejection of impulse noise.

Segment Builder. This block formats the hierarchical data for each layer into the specified number of active segments for that layer.

Time Interleaver. This is a long-delay interleaver to spread the information over time to increase immunity to impulse noise.

Frequency Interleaver. The FITL disperses the data over multiple carriers to minimize signal degradation caused by nulls in the frequency response of the transmission environment.

QAM Mapper. This block performs the QAM constellation mapping for (D)QPSK, QAM16 or QAM64.

Framer and Pilot Insertion. The ISDB-T specification details a frame structure with scattered, continuous and TMCC pilots inserted at various carriers within each symbol. This block manages the pilot insertion dependent on the selected mode (2k, 4k or 8k), and symbol position within a frame.

Detailed Description (cont'd)

IBEQ. An optional in-band equalizer circuit may be specified as a synthesis option. This allows the designer to easily compensate minor phase and gain slope associated with linear filter components on the board.

IFFT. This block performs the Inverse Fast Fourier Transform (IFFT) on the 2k, 4k or 8k carriers. A proprietary architecture is used which yields low Guassian noise, high MER outputs yet utilises low datapath widths. The IFFT also manages the on-air timing of the OFDM symbols by guard interval insertion. An optional windowing function is also included to reduce spurious emissions caused by the OFDM symbol transitions.

Resampler. This block resamples the 8.13 MHz complex IFFT output up to complex samples at the core clock frequency. This provides an ultra-flexible clocking strategy. This block also scales automatically as required to satisfy the selected channel bandwidth.

Baseband-to-IF. This block provides the option to mix the signal up to a higher IF as defined by a software register. This block may be removed using synthesis options if it is not required.

Radio Interface. This block performs some final, register-selectable processing functions to optimise the output for the radio in the target application. An optional processing step provides compensation for the sin(x)/x (or SINC) distortion that is introduced in the DAC. Additionally, the data can be formatted as either twos-complement or offset-binary to suit various DAC devices. In may be formatted for external devices that could take separate I/Q, multiplexed I/Q or a single IF output.

Additional modes are added to support the Analog Devices AD9857/9957 that provides up-conversion, SINC filtering and DAC functions in a single package. The AD9857/9957 device requires that the I/Q data be multiplexed onto a single data bus. The *ad9857_pdclk* input is provided to enable this feature and should be sourced from the AD9857/9957 PDCLK output.

Interface modes are also available to support the Analog Devices AD9789 with RF up-conversion, SINC filtering and DAC functions in a single package.

Register Bank. The register bank provides a simple 32-bit interface for reading and writing registers within the modulator block. Full details of the registers within the modulator core are contained within the full data sheet.

External RAM. Most full-featured implementations will require an external RAM. This can be either SDRAM or synchronous SRAM, allowing implementation on a range of existing platforms.

The SDRAM interface is designed to work with standard interface blocks supplied by FPGA vendors. These interfaces are available to support most SDRAM technologies. The required SDRAM size is 4Mx8.

Alternatively, the CMS0045 also provides direct interfacing to 1MB or 2MB SRAM in 8 16 or 32-bit width.

Serial Programming. The core provides optional programming support for a range of Analog Devices parts, including AD9587/9957 and AD9789 DACs, AD9516 low-jitter clock generator and the ADF4350 low-phase-noise wideband synthesizer.

Principle I/O Description

Global	
clock	Clock input, greater than 57MHz for 8k-mode operation.
ad9857_pdclk	AD9857/9957 Clock.
reset_n	Asynchronous active-low reset input.
Configuration Register Interface	
host_address[]	Host address input
host_wr_data[]	32-bit Host data input
host_rd_data[]	32-bit Host data output
host_chip_en	Active-high, host Chip Select must be high to enable access to the Register Bank
host_wr_req	Active-high, host write enable specifies the current *host_wr_data[]* should be written to the location specified by *host_address[]*.
host_cmd_ack	Active-high host commands acknowledge.
host_irq	Active-high host interrupt line.
Transport Stream Interfaces	
ts_a_data[]	8-bit Transport Stream data input
ts_a_data_valid	Transport Stream data valid input.
ts_a_data_sync	Transport Stream data sync input.
ts_a_data_rdy	Transport Stream path is ready for new byte. (standard TS interface only) Data is transferred when Ready and Valid are asserted together.
ts_a_data_clk	Transport Stream clock input. (PCR re-stamping interface only)
ts_a_data_refclk	Transport Stream reference clock output. (PCR re-stamping interface only)
ts_b_data[]	8-bit Transport Stream data input
ts_b_data_valid	Transport Stream data valid input.
ts_b_data_sync	Transport Stream data sync input.
ts_b_data_rdy	Transport Stream path is ready for new byte. (standard TS interface only) Data is transferred when Ready and Valid are asserted together.
ts_b_data_clk	Transport Stream clock input. (PCR re-stamping interface only)
ts_b_data_refclk	Transport Stream reference clock output. (PCR re-stamping interface only)

Principle I/O Description (cont'd)

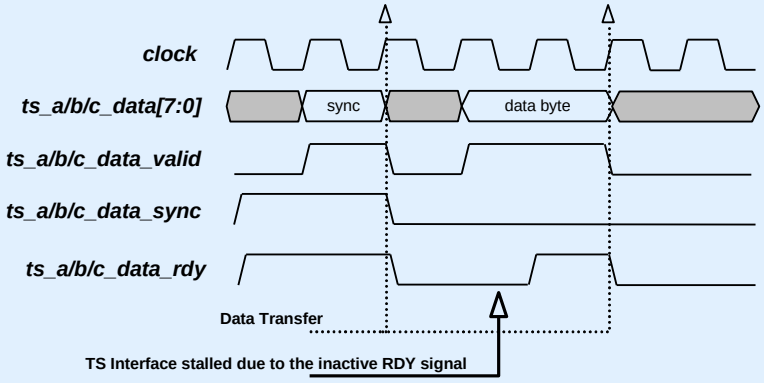
Transport Stream Interfaces (cont'd)	
ts_c_data[]	8-bit Transport Stream data input
ts_c_data_valid	Transport Stream data valid input.
ts_c_data_sync	Transport Stream data sync input.
ts_c_data_rdy	Transport Stream path is ready for new byte. (standard TS interface only) Data is transferred when Ready and Valid are asserted together.
ts_c_data_clk	Transport Stream clock input. (PCR re-stamping interface only)
ts_c_data_refclk	Transport Stream reference clock output. (PCR re-stamping interface only)
Modulator Output Interface	
dac_out_i[]	14-bit Transmit I complex output or IF output in IF mode.
dac_out_q[]	14-bit Transmit Q complex output.
ad9857_txdata[]	14-bit multiplexed data to the AD9857/9957 if used.
ad9857_txenable	Controls the interface timing to the AD9857/9957 if used.
SRAM Interface	
sram_addr[]	Active RAM read/write address output.
sram_data[]	RAM data i/o to be written/read from the RAM.
sram_clk_r	RAM clock output synchronous to core clock.
sram_oe_n	Active-high RAM read enable.
sram_we_n	Active-high RAM write enable.
SDRAM Interface	
ram_cs ram_burst_access ram_burst_size ram_address ram_wr_en ram_rd_en	These command lines interface to the SDRAM controller and queue access requests.
ram_busy ram_available ram_empty	Status lines showing RAM interface availability
ram_wrdata	Write data to SDRAM controller
ram_rddata_valid ram_rddata	Read data from SDRAM controller

Transport Stream Interfaces

The core supports three independent Transport Stream inputs with each being allocated to a specific hierarchical layer.

Standard TS interface:

The basic TS interface uses a ready/valid handshake mechanism, pulling data through the modulator based on the on-air symbol rate for the associated hierarchical layer. This requires the TS data source to be stalled when the modulator core is busy. It also requires external TS rate regulation and PCR adjustment.

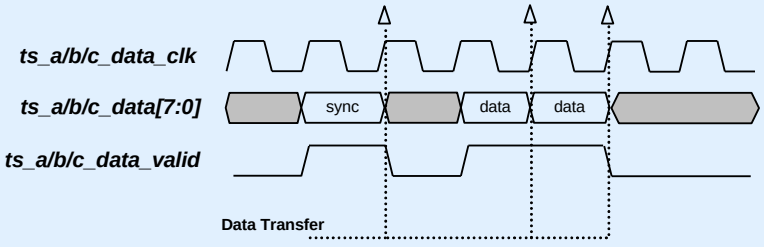


PCR re-stamping TS interface:

In most applications the input stream from the transport multiplexer is provided at a fixed rate and will not support the standard TS interface handshake mechanism. Some form of rate adaption is required. The TS PCR restamping extension core provides a simpler TS interface (compatible with SPI or ASI) to allow data to be input at any rate for the associated hierarchical layer.

The core will be pad the input TS stream with NULL TS packets (or PRBS TS packets) as required and perform any PCR adjustment.

When the PCR restamping extension core is used, an output signal, *ts_a/b/c_data_refclk* is provided to indicate the necessary 188-byte TS byte rate to satisfy the OFDM on-air requirements for the associated hierarchical layer.

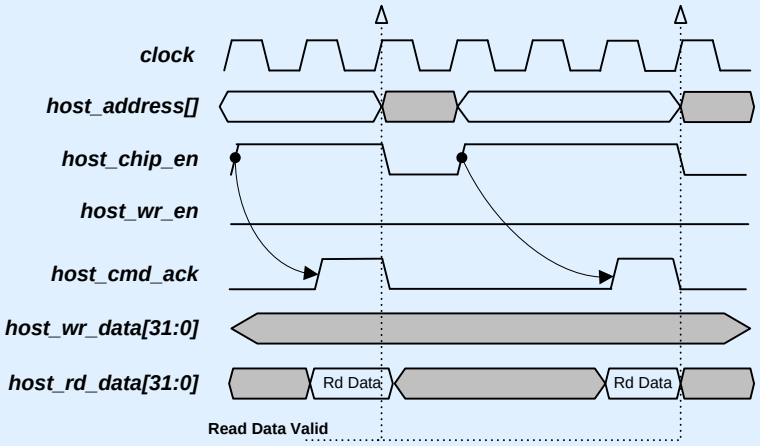


Register Interface

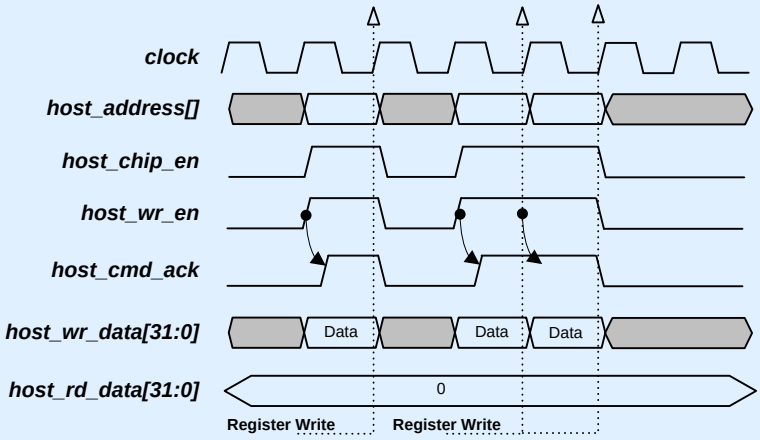
A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

An active-high interrupt line is also available.

Register read access:



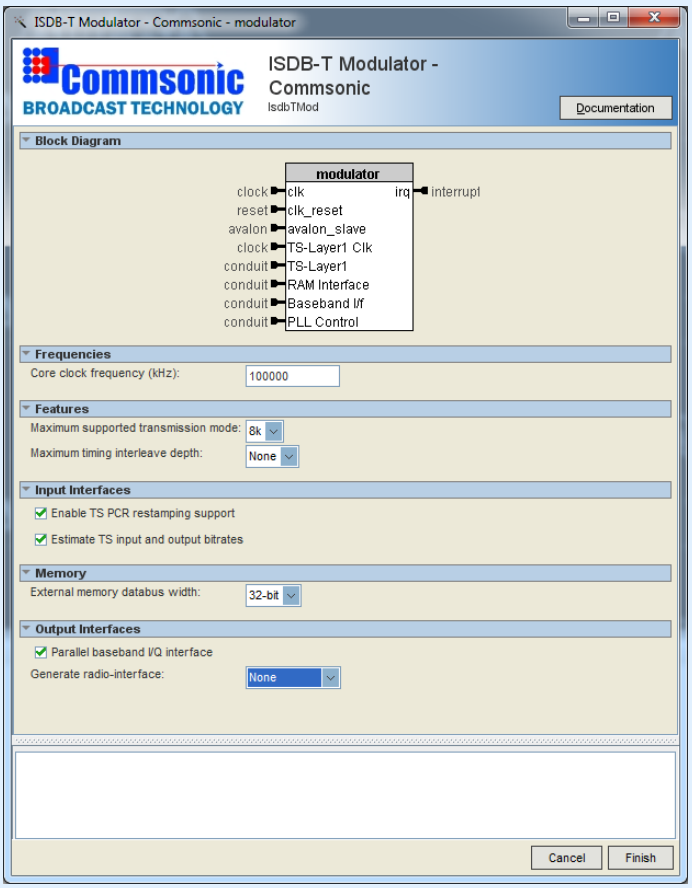
Register write access:



Altera® Megacore®

AMPP℠ Approved | OpenCore® Support | Qsys Compliant

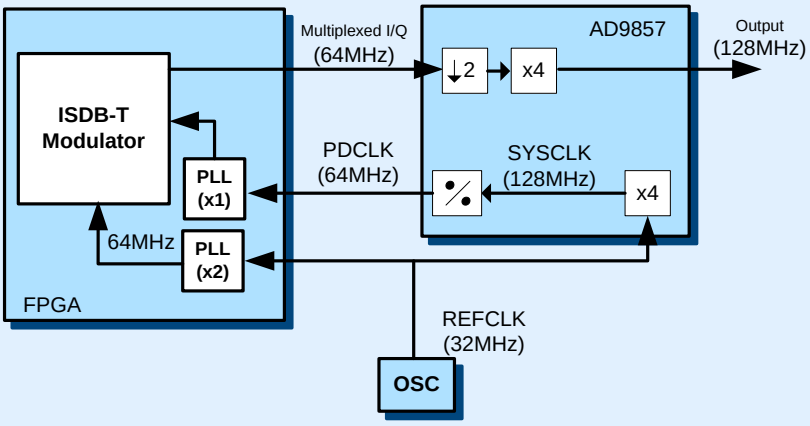
The ISDB-T Modulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.



Example Applications

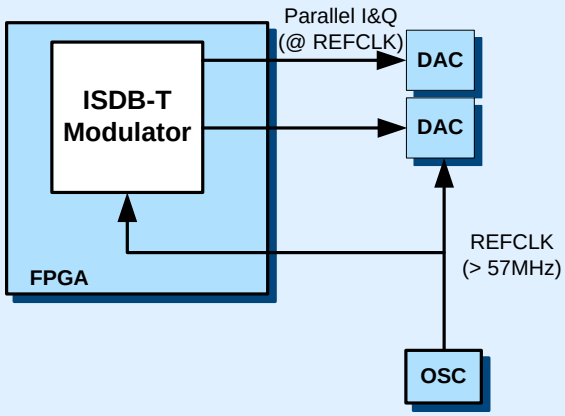
Up-sampled IFFT output using external up-conversion:

This application uses the ISDB-T modulator core with internal interpolation that allows the channel bandwidth to be changed via a simple s/w register change.



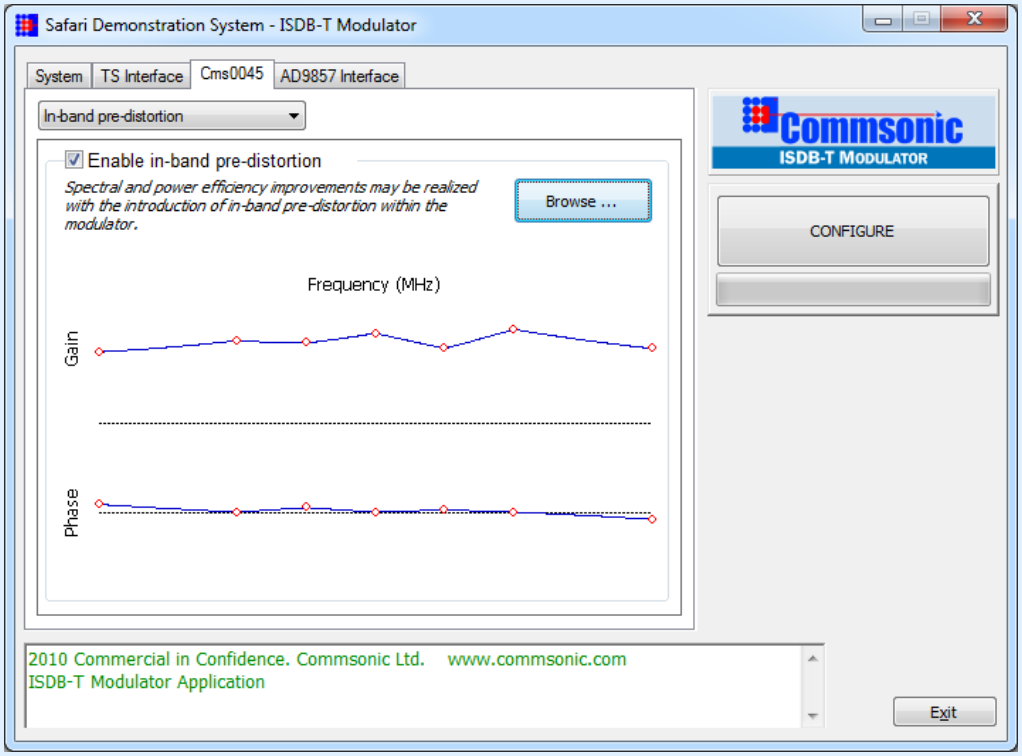
Up-sampled IFFT output using internal interpolation & up-conversion:

This application uses the ISDB-T modulator core with internal interpolation that allows the channel bandwidth to be changed via a simple s/w register change. The ISDB-T modulator internal up-conversion is also used which allows direct connection to external DAC devices

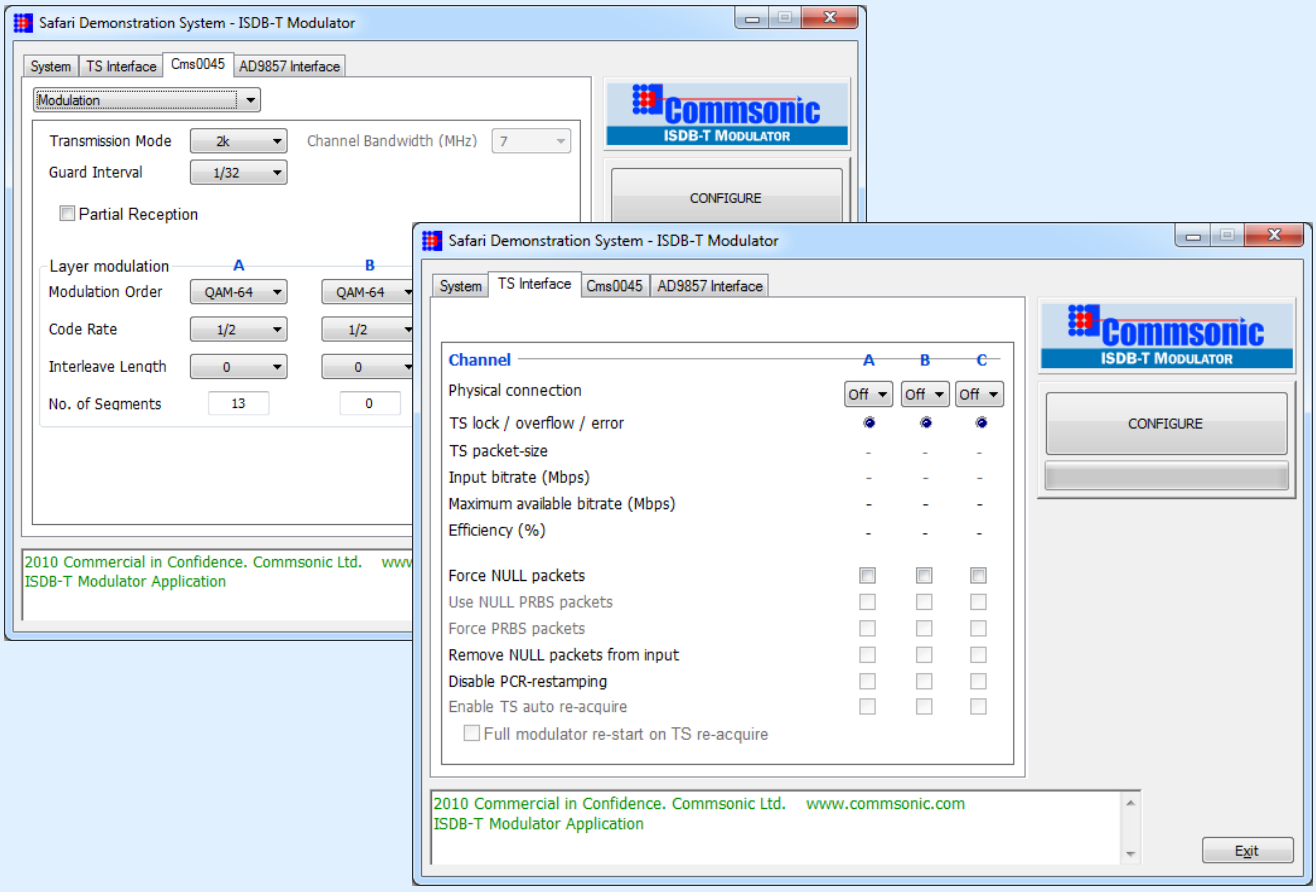


In-band Equalization

The core can be optionally configured to include an in-band equalizer module to compensate for group-delay distortion through the analog and RF amplifier stages.



Evaluation



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, ATSC-8VSB, DVB-C/J.83/A/B/C, ISDB-T, DVB-T/H and DVB-T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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