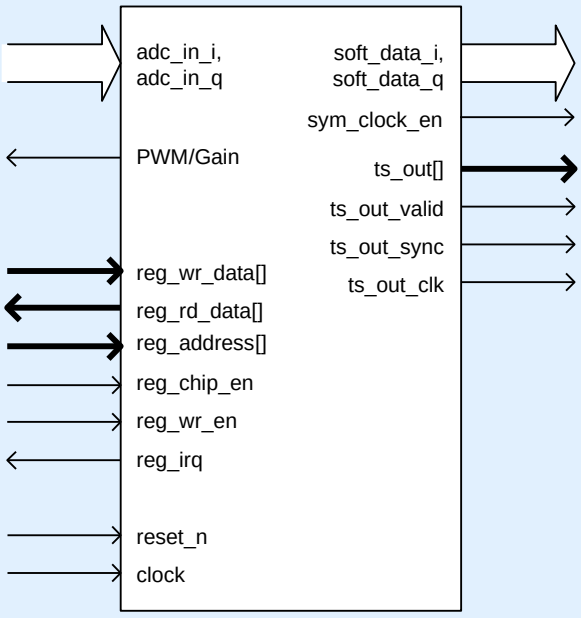
DVB-S/DSNG Demodulator

CMS0048

- Fully compliant with ETSI EN 301 210 and ETSI EN 300 421.
- Optional integrated DVB-S channel decoder.
- Optional DVB-DSNG support.
- Support for an arbitrary range of symbol rates up to 40% of the master clock frequency.
- Two-stage, stepped carrier search provides wide acquisition range.
- Baseband I/Q radio interface incorporating compensation for DC offset and quadrature imbalances.
- Digital decimation and channel filters reject up to +10dBc of adjacent channel interference.
- Fully-digital carrier and clock recovery circuits eliminate the need for an external VCXO.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).



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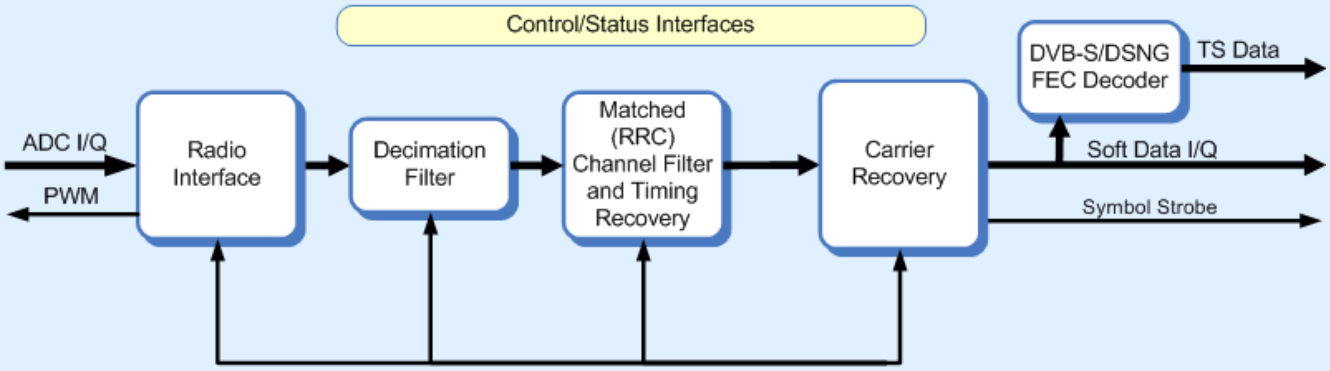
Block Diagram



Detailed Description

The Commsonic CMS0048 DVB-S/DSNG Demodulator is a high-performance (A)PSK demodulator core intended for DVB-S and DVB-DSNG forward link applications.

The demodulator provides soft-constellation outputs together with recovered QAM information suitable for decoding by the integrated DVB-S/DSNG FEC decoder. The TS output stream is smoothed before being output from the core.

Operating symbol rate is programmed from a software register and extends from approximately 40% of the master clock frequency down to an arbitrary low rate that is set through synthesis options. The range would normally be dictated by the application and, in particular, the phase noise characteristics of the radio system.

Carrier acquisition is performed in several stages starting with a coarse, stepped search. The search range and step size are programmed through software registers and can be set to accommodate an arbitrary offset (within the sample rate bandwidth).

Constellation symbols are output as soft decisions after the recovery of carrier phase, symbol timing and gain.

The CMS0048 is provided with a baseband I/Q radio interface compatible with zero-IF and near-zero-IF tuner modules. The interface performs automatic compensation of DC offsets and quadrature imbalances (phase and amplitude).

Tuner Rx gain control is provided through either PDM or parallel gain value outputs. Further stages of gain control are implemented digitally within the demodulator.

The Decimation Filter stage suppresses wideband interference and restricts the sample rate bandwidth prior to matched (RRC) channel filtering and timing recovery. The combined response of the Decimation and Channel Filters allows the CMS0048 to tolerate up to +10dBc of adjacent channel interference at any supported symbol rate.

A single processor at the output of the Channel Filter handles the DVB-S/DSNG demodulation functions – primarily carrier and phase recovery.

The carrier-recovery block corrects the phase and frequency offsets for QPSK, 8-PSK or 16-QAM constellations before delivering soft outputs symbols (unsliced constellation samples) for either external decoding, or to the integrated FEC decoder.

Detailed Description (Cont'd)

Register Configuration

Static configuration and status monitoring is performed through a bank of registers. This would typically be driven from a processor interface connected to a CPU that is embedded on the same device or located off-chip.

Parameters accessible through this interface include:

- Nominal symbol and input carrier frequencies;
- Window and step sizes for the coarse carrier search;
- AGC and PLL configuration and status;
- Estimated signal-to-noise ratio (CNIR).

Important synchronisation events such as the acquisition of symbol timing lock are signalled through the SyncEvents output. Some or all of these signals would typically be connected to the processor interface as sources of interrupt but might otherwise be polled as status indicators.

The Channel and Decimation Filters use hard-wired FIR filter coefficients that are generated during synthesis. FPGA platforms employing more than one Channel Filter configuration would normally store a different netlist for each filter used.

The option of programmable coefficients is available for ASIC and high-end FPGA platforms that have adequate (multiplier) resources.

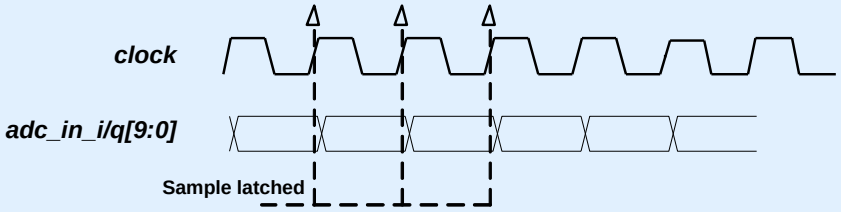
Full details of the register interface are provided in the CMS0048 IP Guide document.

Principle I/O Description

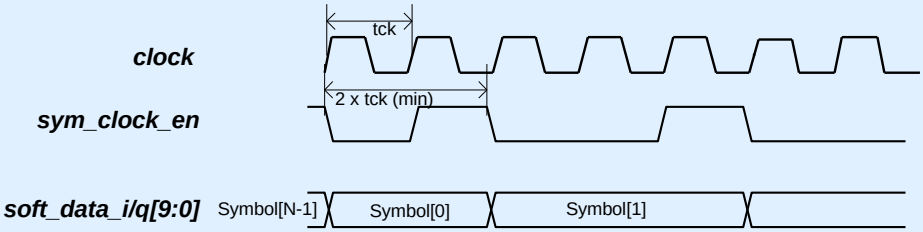
Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0048 register bank.
reg-wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
Radio Interface	
adc_in_i / adc_in_q[9:0]	Complex receive samples at the core master clock frequency. Typically 8-10bits depending upon the tuner filter specification and adjacent channel requirements.
pwm_output	Tuner receive gain control. Typically a single-bit PDM signal but can be configured as a parallel output.
Demodulator Output Interface	
soft_data_i/q[9:0]	Recovered constellation sequence after carrier phase, symbol timing and gain correction. Typically applied as soft input data to a downstream decoder.
sym_clock_en	Qualifier for the samples delivered from the *soft_data_i/q* and *payload_data_i/q* outputs. The average rate is equivalent to the received symbol rate.
TS Interface	
ts_out [7:0]	Decoded TS output stream data.
ts_out_sync	Decoded TS output stream 1st data of packet synchronisation flag
ts_out_clk	TS clock output used to latch *ts_out[], ts_out_valid* and *ts_out_sync.*
ts_out_valid	Decoded TS output stream data qualifier
Others	
clock	Master clock input at a rate not less than 2.5x the maximum operational symbol rate.
reset_n	Asynchronous active-low reset input.
debug_data[31:0]	Complex debug data bus providing status and constellation information from various internal test points within the demodulation chain.
debug_valid	Active-high clock-enable indicating that *debug_data* should be sampled.

Timing Diagrams

Radio Interface:



Soft Constellation Interface:

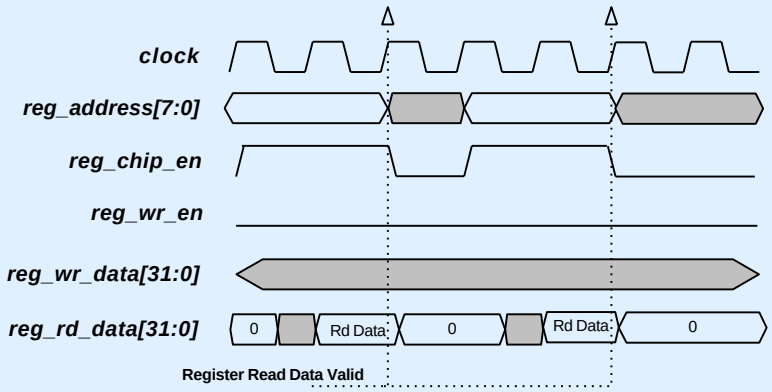


Register Interface

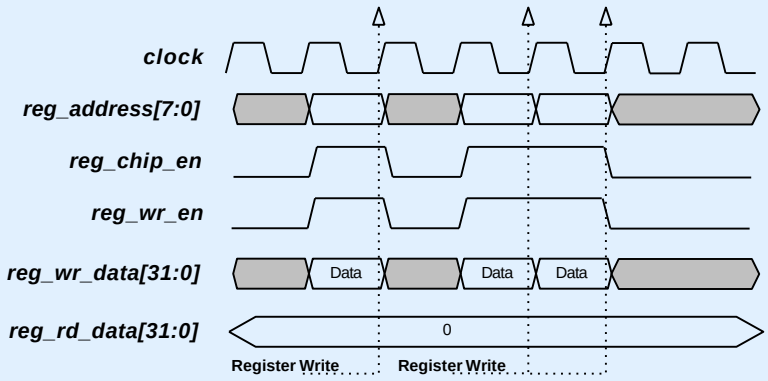
A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

An active-high interrupt line is also available.

Register read access:



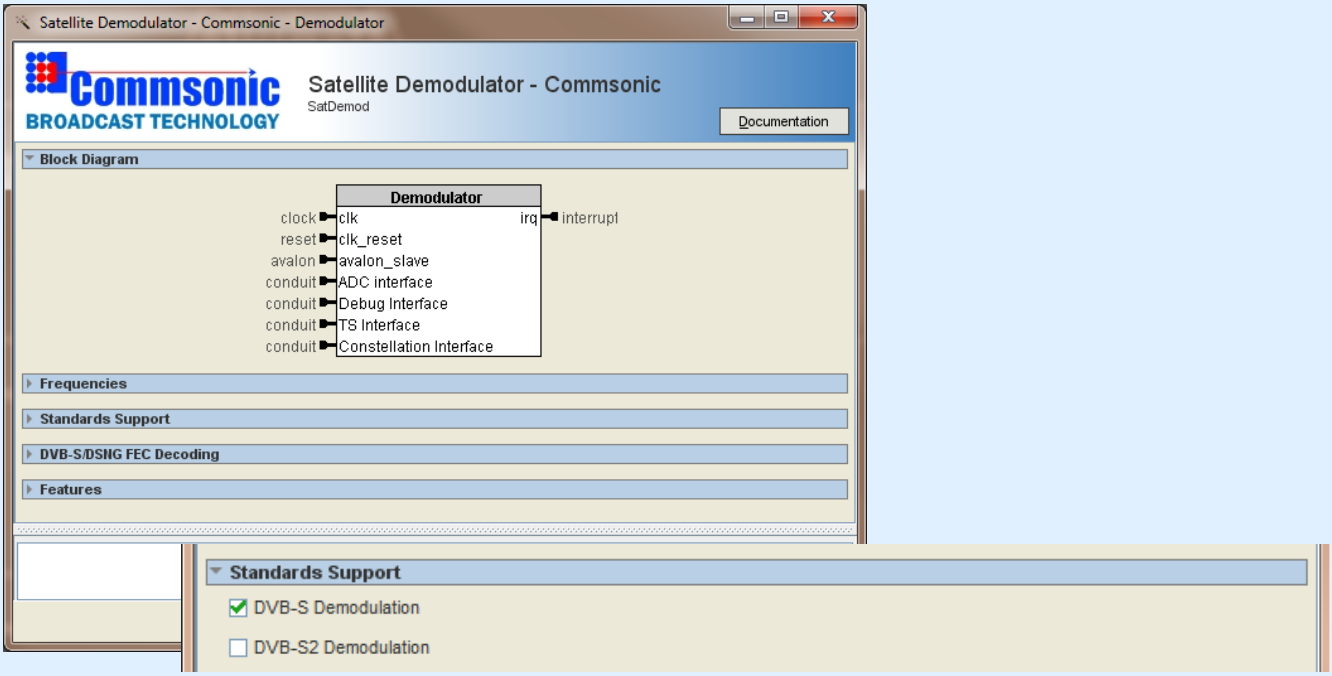
Register write access:



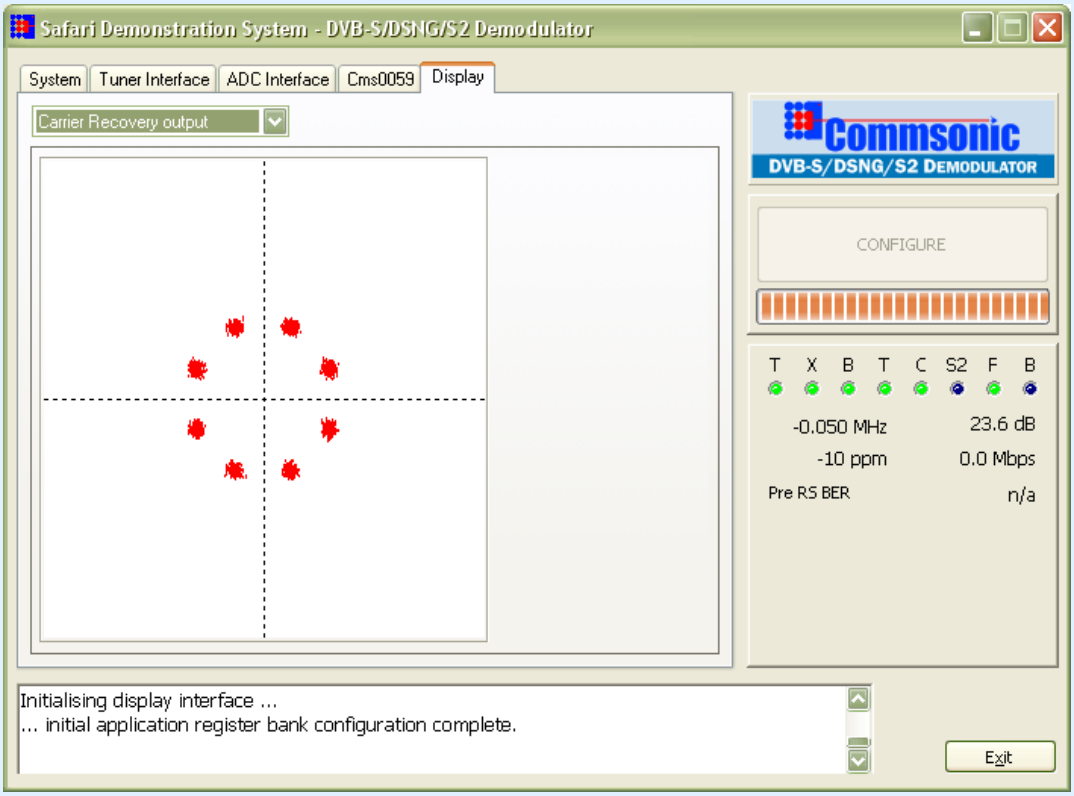
Altera® Megacore®

OpenCore® Support Qsys Compliant

The DVB-S/DSNG Demodulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.



EVALUATION



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, DVB-C/J.83/A/B/C, ATSC 8-VSB, ISDB-T and DVB-T/H/T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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