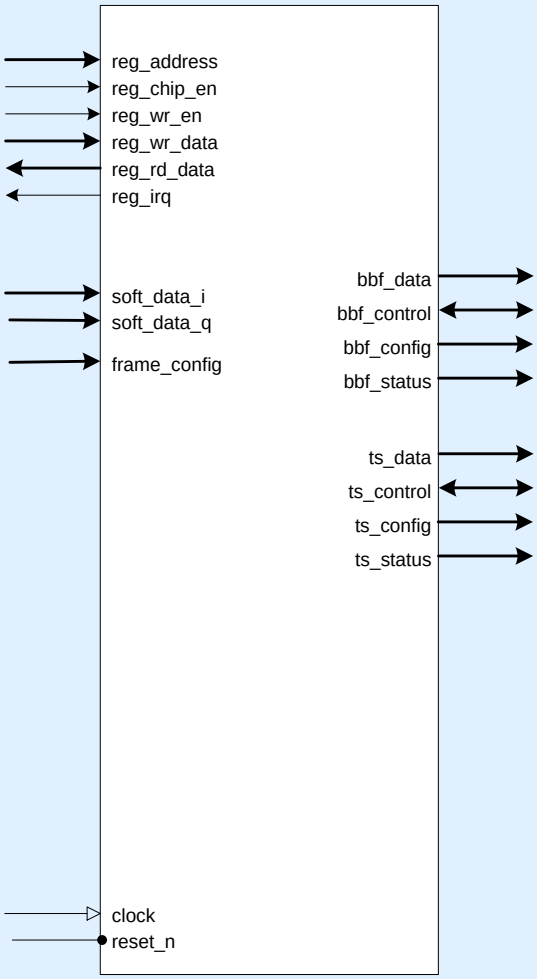
Satellite FEC Decoder

CMS0077

- Fully compliant with ETSI EN-302307-1 / -2.
- The IP core accepts demodulated digital IQ inputs and is designed to interface directly with the CMS0059 DVB-S2 / DVB-S2X Demodulator core.
- Supports QPSK, 8-PSK, 16/32/64/128/256-APSK modes.
- Includes Soft-Decision Slicing, De-Interleaving, LDPC Decoding, De-Scrambling and BCH Decoding.
- Configurable output can support either raw Base-Band Framing data or can generate a constant-rate TS output.
- Synthesis options to tailor resource usage to required performance.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).



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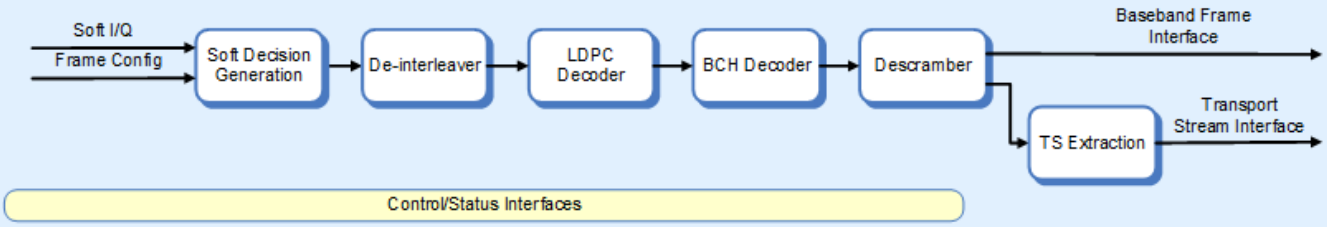
Block Diagram



Detailed Description

The Commsonic CMS0077 Satellite FEC Decoder has been designed specifically to meet the requirements of the DVB-S2 and DVB-S2X advanced wide-band digital satellite standards.

The core provides all the necessary processing steps to convert a demodulated complex I/Q signal into a standard TS output stream.

If configured for ACM operation, the FEC mode can dynamically change on a frame-by-frame basis.

The design has been optimised to provide excellent performance in FPGA devices.

A description of the processing steps follows:

Soft Decision Generator. This block calculates the Log Likelihood Ratios (LLRs) for individual bits encoded in the complex IQ symbols received from the demodulator.

De-Interleaver. Reverses the block-interleave and writes LLR data into the LDPC input buffer.

LDPC Decoder. Performs LDPC decoding of both the main payload data and also the TMCC Header. The decoder uses a modified min-sum algorithm for optimum performance end efficient resource usage.

BCH Decoder. Error-checks the LDPC output and corrects small numbers of residual LDPC errors. Provides reliable detection of uncorrectable decoding errors which are then flagged in the output stream.

De-Scrambling. Reverses the energy dispersal randomisation using the DVB-S2 scrambling polynomial.

TS Rate Adaption. The Decoder output can be optionally configured to produce a constant-rate TS whose byte-rate tracks the off-air symbol rate.

Register Bank. The register bank provides a simple 32-bit interface for reading status registers within the decoder block. Full details of the registers are contained in the IP Users Guide.

Principle I/O Description

General	
clock	Clock input. All input and output is synchronous with this clock.
reset_n	Asynchronous active-low reset input.
Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0077 register bank.
reg_wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
Demodulator Interface	
demod_i	14-bit I complex input.
demod_q	14-bit Q complex input.
demod_valid	Indicates valid symbol I/Q data.
demod_sync	Indicates start of demodulated frame data
demod_pls_code	PLS CODE for the current I/Q frame
demod_flagword	This user-defined data field will be transported through the decoder to the bbf_flagword output. It is pipelined to match the data as it propagates through the decoder and can be used for frame ID or other appropriate frame-linked information.
s2dec_rdy	This output indicates the decoder can accept I/Q data. Input data is transferred when demod_valid = s2dec_rdy = 1. Useful in bursted-data configurations.

Base-Band Frame Data Output	
bbf_data	8-bit frame data output.
bbf_valid	Output indicating bbf_data is valid.
bbf_rdy	BBF transfer enable input. bbf_data is transferred on clock cycles when bbf_valid = bbf_rdy = 1.
bbf_sync	Frame sync marks the first byte of the output frame.
bbf_frame_end	High for one clock cycle following end of data frame.
bbf_ldpc_converged	Indicates the LDPC decoder converged for the current output frame.
bbf_bch_uncorrectable	Indicates the current frame output was uncorrectable.
bbf_plscode	PSL Code for the current output frame.
bbf_flagword	This user-defined data field reflects the value of demod_flagword for the corresponding frame at the decoder input, pipelined to match the data as it propagates through the decoder. It can be used for frame ID or other appropriate frame-linked information.
Transport Stream Output	
ts_data	Byte-wide TS data output.
ts_valid	Indicates TS data is valid.
ts_out_clock	TS byte reference output. Derived from off-air symbol timing. Transfer TS data on cycles when ts_valid = ts_out_clk = 1.
ts_sync	Marks the first 0x47 byte of each TS packet

Output Interface Selection

The decoder output can be configured for either burst mode or constant byte-rate output. This is a synthesis option selected via the Megacore configuration wizard or by VHDL GENERIC settings if directly instantiated.

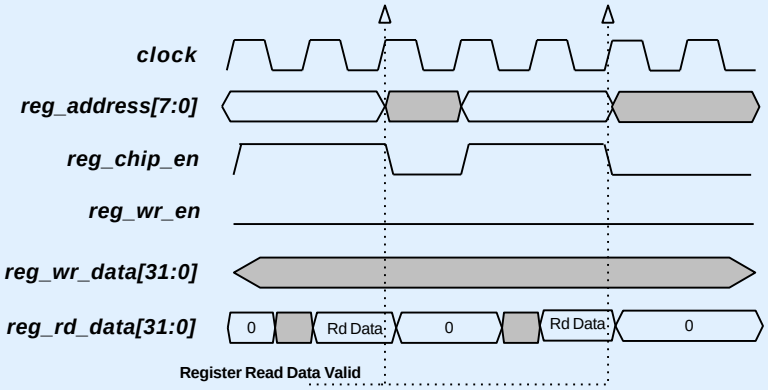
Constant output-rate TS is appropriate for broadcast (CCM) applications. The output rate is linked to the off-air demodulation rate. ts_out_clock regulates the TS data transfers.

Applications based on ACM or time-sharing typically use the BBF output interface to transfer data in minimum time. Output transfers are flexible and the decoder includes at least two frames of FIFO buffer at the output.

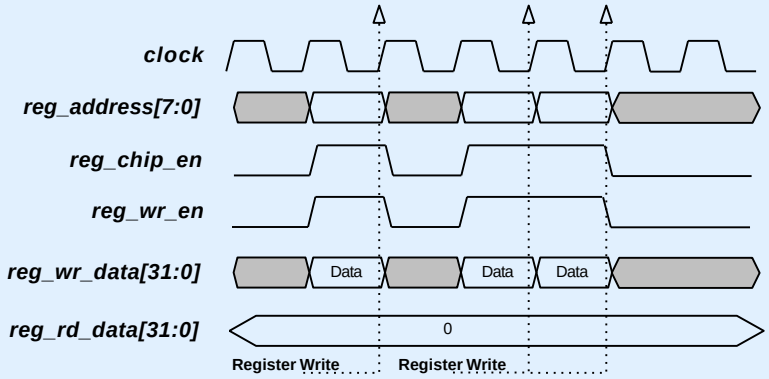
Register Interface

A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interfaced directly with the Altera SOPC/QSYS builder via the Avalon bus using a zero wait-state configuration.

Register read access:



Register write access:



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The Satellite FEC Decoder provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.

About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2/S2X, ISDB-S2, DVB-CID, DVB-C/J.83/A/B/C, ATSC 8-VSB, ISDB-T and DVB-T/H/T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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